Mechanical Behavior of Microelectronics and Power Electronics Solder Joints Under High Current Density: Analytical Modeling and Experimental Investigation

by

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Contents

List of Tables

List of Figures

Abstract

This dissertation focuses on the mechanical reliability of microelectronics solder joints under high density electric current stressing. It contains both experimental and analytical modeling parts.

In the experimental part, high density current stressing experiments were conducted using flip-chip and Ball Grid Array (BGA) test vehicles. In addition to electromigration, thermomigration is also studied and observed. The major failure mechanism is identified as the void nucleation and growth due to the combined effects of electromigration and thermomigration. Nano-indentation tests show that the elastic modulus of a solder joint degrades during current stressing. A Pb phase coarsening model that includes the influence of current density is proposed. The Moiré Interferometry technique is used to measure the in-situ displacement evolution of BGA solder joints under electric current stressing.

In the analytical modeling part, a diffusion-mechanical coupled stress-current density constitutive model for solder alloy under electromigration is presented. The constitutive model is numerically implemented into FEM code to simulate the displacement fields of the BGA lead-free solder joints under current stressing. Despite all of the assumptions and simplifications employed in the simulation, it predicts reasonably close displacement results to the Moiré Interferometry experimental results in both spatial distribution and time history evolution. This indicates that the electromigration model is reasonably good at predicting the mechanical behavior of lead-free solder alloy under electric current stressing.

Chapter 1

Introduction

1.1 Motivations

The development of micro electronics technology is driven by the insatiate demand to for miniaturization. Electrical power can be controlled very efficiently with semiconductor technology. The power range commanded by converters now extends from micro-VA to several hundreds of MVA (Van Wyk and Lee 1999). Among these new power devices, Insulated Gate Bipolar Transistor (IGBT) devices are becoming more accepted and are increasingly being used in various applications. Thus predicting the long-term reliability of IGBT power electronics is highly demanded (1994). Since there is significant power dissipation in the system that needs to be removed through electronic packaging, thermal and thermo-mechanical management is critical for power electronics modules. All interfaces in the module could be locations of potential failures (Auerbach and Lenniger 1997). Since the system carries very high current, high current induced mechanical failure mechanisms must also be taken into consideration for predicting long-term reliability.

Wire bonding is the dominant IGBT packaging technique used today; emitter bonding wire lifting is reported as the most important failure mode (Wu et al. 1995b). The press-pack technique was developed to avoid this weakness. Another attractive packaging technique for next generation power packaging is surface mount technology,

such as flip-chip packaging, which can provide better electrical performance and much larger real estate for high IC density(Xiao et al. 2001;Paulasto-Krockel and Hauck 2001;Liu et al. 1999b). One example is FlipFET™ packaging technology by International Rectifier. At the same performance level, their power Metal-Oxide Semiconductor Filed-Effect Transistor (MOSFET) using flip-chip packaging technique provides much smaller size and an ultra low profile, significant reduction in static drain-to-source on-resistance, equivalent or better thermal performance, and virtual elimination of package parasitic devices (Schofield et al. 2003). In flip-chip power semiconductors and evolving system-in-package power processors, each solder joint carries very high electric current density.

In microelectronic packaging, the trend in flip-chip and ball grid array (BGA) package is to increase the I/O count. This drives the solder joints to be smaller in size and, thus, carry higher current density. As projected in the National Technology Roadmap for Semiconductors, up to 10,000 interconnects may be needed on a chip of 1×1 cm^2 (1997). Thus the size of the solder joint has to be reduced to below 50μm. The current density for a single solder joint could be well above $1x10^4 amp/cm^2$ (Lee et al. 2001a). International Technology Roadmap for Semiconductors (ITRS) is another undertaking working to assess the requirements for microelectronics for the next 15 years, with companies from U.S., Japan, Taiwan, South Korea, and several European nations cooperating on the project. The projection in ITRS 2001 edition shows that in both near-term and long-term, core voltage will decrease; the chip power consumption and package I/O count will increase. For example, for a chip in high-performance category (>$3000 high-end workstations, servers, avionics, supercomputers), the core voltage is projected to decrease from 1.1v to 0.4v by 2016; on the other hand, the power consumption in a single chip is

projected to increase from 130 watts to 288 watts, and the I/O count is projected to increase from 1700 to 7100 by 2016 with no change in chip size (2001a). The dramatic decrease in core voltage and increase in power consumption will dramatically increase the current level in each solder joint. The increase in I/O count leads to reduction in the pitch and size of solder joint. ITRS projects that the bump pitch in flip-chip assembly will decrease from 160 μm or greater today, to 70 μm by the end of the period for high I/O and high power chips (2001a). Higher current level and smaller bump size leads to higher current density in each solder joint.

The high current density in the solder joints is a known reliability concern for next generation power electronic packaging and high density microelectronic packaging (Lee et al. 2001a;Lee and Tu 2001;Ye et al. 2002a;Ye et al. 2002b;Ye et al. 2003a;Ye et al. 2003b;Ye et al. 2003a;Ye et al. 2003c). A physical limit to increasing the current density in both microelectronics and power electronics is electromigration. Electromigration in interconnect metal lines is the major failure phenomenon in ICs, but is a seldom recognized reliability concern for solder joints due to their relatively large size and low current densities. Most research has focused on electromigration of thin metal lines (Agarwala et al. 1972;Attardo and Rosenberg 1970;Black 1969;Blech and Kinsbron 1975;Blech 1976;Hu and Harper 1998;Knowlton et al. 1995;Lee and Tu 2001;Li et al. 1999;Lloyd 1999b;Tang 1994;Tu 1992b;Korhonen et al. 1993;Rzepka et al. 1997;Kirchheim 1992;Gleixner and Nix 1996;Sarychev and Zhinikov 1999), and there is little knowledge base on electromigration of present day solder interconnects (Brandenburg and Yeh 1998;Lee et al. 2001a;Lee and Tu 2001;Liu et al. 2000a;Liu et al. 1999a;Tang and Shi 2001). Beside electromigration, thermomigration due to the thermal

gradient within the solder joint, which is caused by joule heating, is another reliability concern during high current density stressing (Johns and Blackburn 1975;Roush and Jaspal 1982;Ye et al. 2003b). The damage mechanics of solder joints under high electrical current density has never been studied before in a formal research project. An extensive literature survey in the subject indicates that there is a big vacuum in this field. This work attempts to fill the vacuum. The work provides the basic understanding of the failure mechanism of solder joints under high density current stressing, mechanical property degradation as observed by nano-indentation, displacement evolution measurement with the Moiré Interferometry technique, and verification of a material constitutive model for solder alloy under current stressing by finite element (FE) simulation.

1.2 Background and Literature Survey

Failure Modes of Power Electronic Packaging

All power devices have finite on-state voltage drops when conducting the on-state currents and finite switching times during turn-on and turn-off. These effects result in significant power dissipation in the system that needs to be removed through electronic packaging. As reported, in a typical IGBT based motor drive, 4% of the controlled power is dissipated as heat within the device (He et al. 1998a). Thus thermal and thermal-mechanical management is critical for power electronics modules. The failure mechanisms that limit the number of power cycles are caused by coefficient of thermal expansion mismatch between the materials used in the IGBT modules. All interfaces in

the module could be locations of potential failures (Auerbach and Lenniger 1997). Several researchers conducted experiments to estimate the long-term reliability and the failure modes of power semiconductor modules (Wu et al. 1995b;Wu et al. 1995a;He et al. 1998b;Nicoletto et al. 1999).

1.2.1 Existing and Developing Techniques of Power Electronic Packaging

The failure modes of power electronic modules are dependent on the mounting technology used. Different packaging techniques used in mounting power electronics are reviewed in this section.

A. Wire bonding technique

Wire bonding (Figure 2a) and press pack (Figure 2b) are two different mounting techniques with different failure modes. The wire bonding technique has been widely used in power electronic packaging for many years and it is still the most popular technique used in the state-of-the-art power modules. Inside these power modules, bonding wires (Al wire) are used to interconnect power devices. Usually this kind of packaging comprises two circuit layers. On the bottom a direct copper bonded (DCB) substrate is soldered on a heat sink, with the power devices soldered on the substrate. A FR4 printed circuit board (PCB) is mounted on top of the power devices and serves as driver, sensors, protection circuits, and control circuits. The package is finally filled with silicone gel and housed in epoxy. Figure 1 shows a typical wire bonding power electronic packaging.

B. Pressure Contact technique

The wire bonding technique has certain weaknesses in reliability. One main failure mechanisms observed in service is emitter wire lift-off and cracking in the solder

layer. To avoid these problems, the pressure contact technique (press pack or flat pack), previously used for Gate Turn-Off (GTO) thyristor, is getting more interest in IGBT packaging. This is especially true in the applications such as automotive and railway traction, where both high power and long life span are important issues (Nicoletto et al. 1999). As illustrated in Figure 2b, bonding wires and solder layers are eliminated in this technique. The electric contact is obtained by pressing the IGBT chip and diode between two high-planarity copper discs. Between the silicon chips and copper plates are molybdenum washers, which serve as thermal compensating buffers.

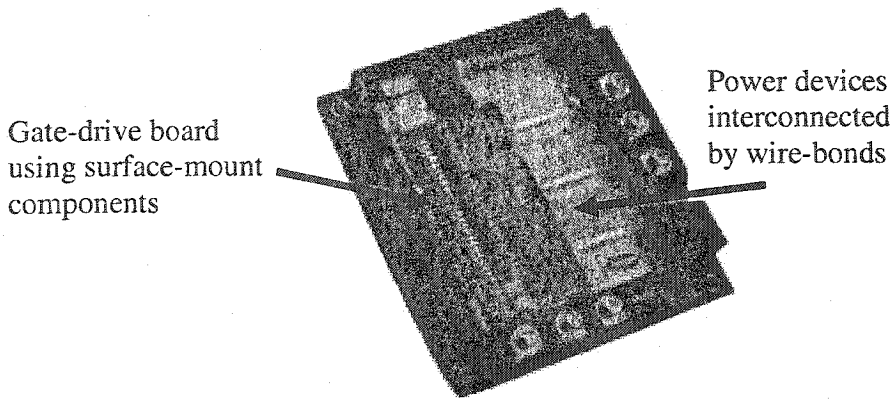
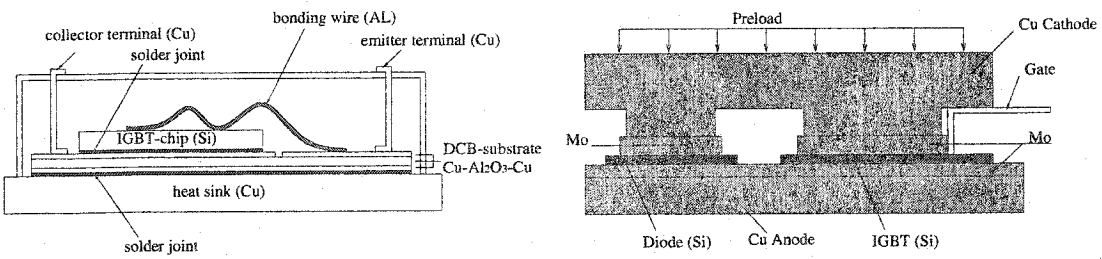


Figure 1 A typical wire bonding packaging (after Wen, S.(Wen 2001))



(a) Scheme of Wire Bonding IGBT module

(b) Scheme of Press-Pack IGBT module

Figure 2 Schemes of wire bonding and press pack packaging

C. Flip-Chip Technique

Surface mount technology especially flip-chip technology are widely used in the integrated circuits (ICs) packaging. The flip-chip technique can provide very high density

input and output interconnections for ICs. It is low-cost and high reliability. The application of the flip-chip technique in power electronic packaging eliminates wire bonding interconnects and, instead, utilizes solder joint interconnects that are capable of carrying large currents for interconnecting devices. The low-profiled solder joints introduce negligible parasitic inductance and capacitance at the connections compared to conventional wire bonding connections, thus providing less noise and better electrical performance. Also, the use of an underfill dielectric material between the devices and substrate helps to achieve protection and stress reduction in the devices as well as improve heat transfer (Liu et al. 2000b).

Liu and Lu (Liu and Lu 2001) reported a chip scale package, termed Die Dimensional Ball Grid Array (D^2BGA, Figure 3), for making area bonded Chip-scale packaged (CSP) power devices. These surface-mountable CSP power devices allow the implementation of three-dimensional approaches for packaging power electronics modules that have high levels of integration with power semiconductor devices, gate drive, and control circuitry for a wide range of power electronics applications. Liu et al. evaluated the static electrical performance of their D2BGA chip-scale packaged IGBT, commercial packaged IGBT, and wire bond module using SONY Tektronix 371 programmable high power curve tracer (Liu et al. 2000b). They claimed that D^2BGA IGBT has the lowest voltage drop and on-state resistance. The switching characteristics for IGBTs are: switching times, switching energy, and stray inductance. Stray inductance causes turn-off over-voltage spikes and turn-on voltage drops. Liu et al. compared the voltage overshoot characterized by switching test. They reported that the flip-chip module had about 8.7% voltage overshoot, while the commercial IGBT device and wire

bonding IGBT module had about 14% and 20.8% voltage overshoot, respectively. This could be explained by the fact that the low profiled solder interconnects have significantly lower parasitic inductance compared to bonding wires (Liu et al. 2000b).

The researchers of Center for Power Electronics Systems at Virginia Tech reported the use of flip-chip technology to build Integrated Power Electronics Modules (IPEMs) (Liu et al. 1999b). They claim that their IPEM permits higher frequency operation with increased conversion efficiency, while reducing component size and module cost. This IPEM package is a multilayer structure (Figure 4). The bottom layer, a direct-bond copper substrate, is used for attaching power chips. The chips are embedded in a thermally conductive dielectric layer. Triple-stacked solder joints are used as the interconnection between the power devices and the flexible substrate with the circuit pattern for gate-drive components. The devices are encapsulated using underfill polymer materials to reduce the thermo-mechanical stresses imposed on the solder joints.

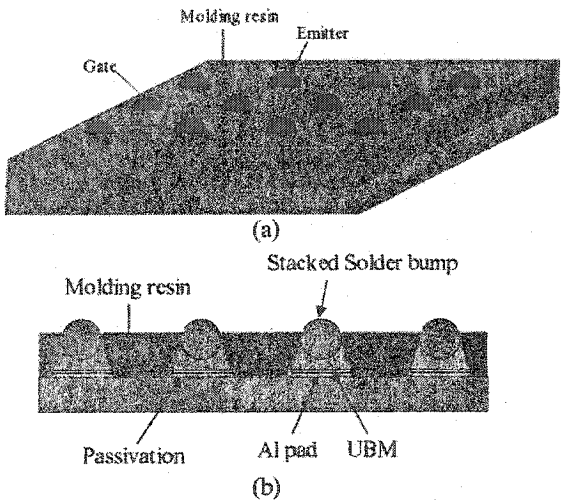


Figure 3 (a) The structure and (b) the cross sectional view of D^2BGA chip-scale packaged power device (after CPES, Virginia Tech (Liu and Lu 2001))

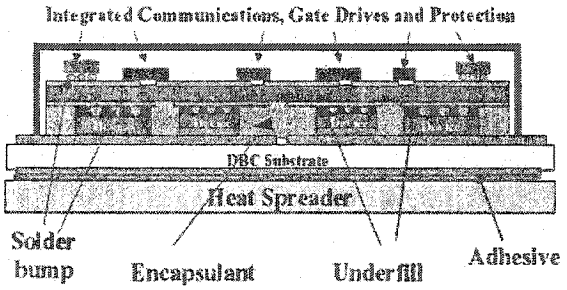


Figure 4 Schematic structure of flip-chip IPEM (after CPES, Virginia Tech, (Liu et al. 1999b))

There are several commercialized power electronic modules utilizing the flip-chip technique. One example is FlipFET™ MOSFET by International Rectifier (Figure 5a). In this technique, all the terminals of a HEXFET® device are positioned on the same face of the die, which enables the development of wafer scale packaged (WSP) MOSFETs. They claim that at the same performance level, this power MOSFET provides much smaller size and an ultra low profile (<0.8 mm), significant reduction in static drain-to-source on-resistance, equivalent or better thermal performance, and the virtual elimination of package parasitic devices (Schofield et al. 2003). Another example of using flip-chip packaging technique in mounting power modules is the PowerTrench® BGA MOSFET from Fairchild Semiconductor Corporation (Figure 5b). The advantage of this package includes: reduction in size, ultra-thin profile (<0.7mm), outstanding thermal transfer characteristics, ultra-low static drain-to-source on-resistance, and high power and current handling capability (2003).

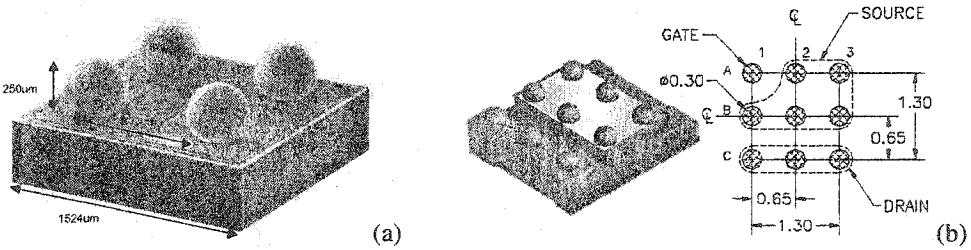


Figure 5 (a) the FlipFET™ MOSFET package from International Rectifier (after Schofied (Schofield et al. 2003)) (b) PowerTrench® BGA MOSFET from Fairchild Semiconductor (courtesy to Fairchild Semiconductor Co.)

With all the outstanding advantages flip-chip technique provides, it is the future packaging technique for high speed, high performance power modules, and IC modules.

D. Other Packaging techniques

There are other power electronic packaging techniques reportedly under development, such as GE's thin-film power overlay technology, Virginia Tech's metal-posts interconnected parallel-plate structure, et al. (Wen 2001).

1.2.2 Failure Modes of Wire Bonding Packaging

A. Emitter Bonding Wire Lifting Failure

For wire bonding IGBT modules, the emitter bonding wire lifting is reported as being the most important failure mode (Wu et al. 1995b). In Wu's research (Wu et al. 1995b), more than forty 300A/400A 1200V IGBT modules were subjected to a power cycling test. It was reported that no tested modules could pass 10^6 power cycles. Wire lifting failure occurred in about 70% of the tested modules. Wu et al. believe that the poor bonding pressure and contamination may lead to low fracture strength at the bonding interface. Moreover, bonding wires are subjected to a tensile stress due to the temperature fluctuation during power cycling. Longer wire is subjected to higher tensile stress. This tensile strength also affects the bonding strength. Lambilly and Keser (de Lambilly and Keser 1993) tested the reliability of power IGBT modules with the power cycling method. They also observed lifted wire bonds. The Al wire has much larger CTE and expands during heating. They concluded that when the stiffness of the wire and potting material prevent the deformation of the wire, the whole strains are converted to large stresses on the bond area, which is sheared from silicon. This can be amplified by the stiffness and the large CTE of the potting material. They indicate that without stiff potting material,

better performance of bonding wire can be achieved. In Cova and Fantini's research (Cova and Fantini 1998), some medium power devices were subjected to power cycles. The module is placed in a thermally controlled chamber to establish the ambient temperature by forced air ventilation, from 0 to 150°C. Emitter bonding lift-off was the main failure mechanism. Cova and Fantini (Cova and Fantini 1998;Cova et al. 1999) claim that the degradation of the die attach is probably the root cause of the failure mechanism. They also claim that the thermal excursion ΔT may be the cause for damage of the soldering layers and bond wires and the power cycling life time is exponentially related to ΔT.

Another research project by Auerbach and Lenniger (Auerbach and Lenniger 1997) also indicates that the predominant failure mechanism is the lift-off of the bonding wires. But the solder degradation between the substrate and copper baseplate as well as the solder degradation between the chip and the substrate are also important failure mechanisms. Their conclusion is similar to that of Auerbach and Lenniger's. They concluded maximum number of power cycles decreases with increasing temperature swing. They also found that the medium junction temperature is very important for determining the maximum number of power cycles that a module can stand. Lower medium temperature leads to higher power cycling stability.

B. Solder Degradation

Solder degradation may cause different types of failure. IGBT modules are multilayered structures. Silicon die is soldered on the DCB substrate, and DCB is soldered on the copper heat sink. The substrate and heat sink have much larger CTE than the silicon die. This CTE mismatch requires the die bond to be compliant to prevent large

stress in the silicon die. Soft solder is more suitable for use here, since it has a low modulus of elasticity, low yield strength, and relatively high ductility. Thus it allows plastic deformation of the bond. Alternatively, less compliant solder may be used if a buffer layer (such as Molybdenum) is used between the substrate and die (Evans and Evans 1998).

A significant amount of heat dissipated by the IGBT modules needs to be removed through this sandwiched structure. Solder degradation at any location increases the thermal resistance from the silicon module to the heat sink. Cyclic temperature shifts during operation produce cyclic shear strains in the die bond due to the CTE mismatch between layers and the spatial temperature gradients. This eventually produces cracking due to fatigue, which lowers the critical capability of the bond to transfer heat generated in the die (Lee 1993;Olsen and Berg 1979;Pecht et al. 1994). Evans (Evans and Evans 1998) states that spatial temperature gradients and transient thermal effects play significant roles in die bond fatigue failure. Fatigue cracks initiate rapidly in solder. They generally begin at the corner or edge of the die (the point of maximum shear strain) and grow through the die bond. In a die bond of uniform thickness, the crack growth is expected to proceed toward the neutral point or center of the die. The loss of die bonds increases the die temperature, and effectively reduces the safe operating area of the IGBT. Thus the power transistor eventually fails from catastrophic burn-out or secondary breakdown. Evans and Evans (Evans and Evans 1998) used 133 power transistors in power cycling intermittent operating life test. Their analysis shows that increasing die bond thickness has a significant role in improving the cyclic life of the die bond. Die bond thickness varies substantially between devices and may not be uniform under a

single die. This non-uniformity influences the device life by increasing strain concentration and influencing crack growth. In the test by Wu, et al. (Wu et al. 1995a), the forming and growing process of voids and cracks in the solder layer of fine-prepared IGBT cross sectional samples was quasi-dynamically observed during thermal cycling test. It indicated that void free solder material is important in order to produce high reliable power modules. In another power cycling test, Wu, et al. (Wu et al. 1995b) observed that the local overheat burn-out failure due to big voids in the solder layer. In the thermal cycling test by Shaw, et al. (Shaw et al. 2000), each test vehicle was inspected by a high frequency ultrasonic C-scan imaging technique. Shaw, et al. then observed the crack initiation and subsequent growth. Since the voids are almost unavoidable in any solder joints, Zhu (Zhu 1999) discussed the thermal impact of different types solder voids using finite element method.

C. Cracks in Silicon Die and Substrate

Large semiconductor devices can be subjected to significant mechanical stress resulting from the CTE mismatch between different layers of devices. In these layers, silicon die and Al_2O_3 or AlN (used as an insulator in DCB substrate) have a small CTE. On the other hand, the CTE of most metals is several times larger. Due to the bimetal effect, when this multilayer structure is subjected to temperature changes, thermal stresses are developed, which results in bending deformation. These stresses may cause the brittle silicon and Alumina to crack (Wen 2004).

Wu, et al. observed thermal stress induced IGBT chip crack failure in the power cycling test (Wu et al. 1995b). The cracks in silicon chip and Alumina were also observed in Wu et al.'s (Wu et al. 1995a) thermal cycling test of cross sectional samples

of IGBT module. A simple simulation by Wu, et al. (Wu et al. 1995a) shows that the stresses in the copper substrate and the copper heat sink are compressive, and the silicon chip and Alumina layer are subjected to high tension stresses, which cause them to crack.

It is also reported that the residual stress during manufacturing may cause mechanical failure or change the operational characteristics of power modules (Colbourne and Cassidy 1991). Manufacturing requires heating the components above the melting point of solders. Because of the CTE mismatch between layers, significant residual stresses develop during cooling. This affects the reliability of the power module during operation. By using the piezospectroscopic techniques, the absolute magnitudes and spatial distributions of time-dependent thermal residual stress on the surface of silicon die were measured by several researchers (He et al. 1998a;He et al. 1998c;He et al. 1998b).

D. Electromigration in Bonding Wires

The electro-migration failure in bonding wires is reported by Wu et al (Wu et al. 1995b). The high temperature plays an important role in thick wire electro-migration even when the current density is low.

E. Surface Degradation in Emitter Bonding Pads

Surface degradation in emitter bonding pads was observed in Wu, et al's test (Wu et al. 1995b), and it could be accelerated by thermo-mechanical stress due to the different CTE of Al and Si. It was found that the metallization surface became rough and hillocks formed because of recrystallization and electro-migration during power cycling. This process could be accelerated by thermo-mechanical stress due to the CTE mismatch. Wu,

et al. found that chip passivation or polyimide coating could improve IGBT Al metallization degradation.

1.2.3 Reliability of Press-Pack Packaging

By removing the wire interconnections and solder layers, the press pack technique avoids the frequently occurring failures in wire bonding modules, such as solder cracking and wire bonding lift-off. Nevertheless, specific failure mechanisms may arise. Although the main failure causes of the conventional wire bonding technology are well understood, the failure mechanisms of press-pack IGBTs are still under investigation. There are few reports on the reliability of press pack packaging compared to the extensive literatures on failure modes of wire bonding packaging.

By removing the solder layer, this technique eliminates the residue stress on each material, but raises the concern of mechanical damage caused by pressure force. Hideo Matsuda, et al (Matsuda et al. 1997) performed stress analysis and examined the electrical characteristics for both planar and trench gate structures under the pressed emitter electrode condition. There was no mechanical damage or change in electrical characteristics observed. Nicoletto et al. (Nicoletto et al. 1999) did accelerated testing of press pack IGBTs. They designed a testing rig for power cycling of a single chip under controlled contact pressure conditions. Two flat steel probes are used to press the IGBT chip and a 3 KN pneumatic actuator was used to apply the required force. Cova et al (Cova et al. 1999) did preliminary failure analysis of press pack device by using this testing rig and FEM simulation. Their analysis confirmed the early postulated mechanisms (Pirondi et al. 1998) that pressure non-uniformity and thermal cycling of

materials with CTE mismatch can cause fretting on the emitter pads and thermal fatigue of metals.

Due to the lack of failure data of press packed IGBTs from the field, more research work is needed to understand their failure mechanisms.

1.2.4 Reliability of Flip-Chip Power Modules

Compared to the wire bonding and press pack techniques, flip-chip packaging is the next generation packaging technique for power modules. Most flip-chip packaged power modules are still on the test stage.

Liu, et al. (Liu et al. 2000b) performed some tests to evaluate the reliability of flip-chip power modules. They show that the flip-chip technique provides an additional thermal path – the top solder joints. This makes three-dimensional cooling possible, while the wire bond modules are limited to one-directional heat dissipation. The main thermal path is the back of the power device. Due to the very short length and large contact area of a solder joint, the solder joint interconnection itself is a good thermal path. Thermally conductive encapsulant is the third thermal path, which helps dissipate heat from power chips. They conducted thermal cycling test to verify the reliability of the D^2BGA CSP and IPEM packages. Two evaluation criterions were used. One is the increases of electrical resistance of solder joint interconnections, the other is the change of collector emitter voltage drop, $V_{ce(sat)}$. The specimens were subjected to a temperature change of 0°C and 100°C with the rate of cycle/30 minutes. The packages were dynamically tested for functionality during the power cycling at both high temperature (100°C) and low temperature (0°C). They reported that $V_{ce(sat)}$ did not obviously increase before 3600

cycles. Until 4800 cycles, Vce(sat) has a 16% increase in the original value. There was no resistance increase of the solder joint after 3600 cycles.

By introducing the flip-chip technique into power electronic packaging, the reliability of solder joints becomes essential to the reliability of power modules. There is already extensive literature addressing the reliability issues of solder joints in microelectronic packaging. Most of research focuses on the thermo-mechanical reliability of the solder joints under thermal and mechanical loads. With the continuing increase of electric current density in solder joints, the behavior of solder joints under high density current stressing is also becoming a reliability concern.

The flip-chip packaging technique enables the new generation of power modules to combine excellent thermal transfer characteristics, high current handling capability, ultra-low profile packaging, low gate charge, low static drain-source on-resistance, and much reduced parasitic inductance and capacitance. At the same time, the solder joints in these packages carry extremely high current density. For example, the International Rectifier's IRF6100 HEXFET® Power MOSFET, which has a small footprint of only $1.5\times1.5mm^2$ (Figure 5a), is designed to handle a drain-source voltage of 20V, a continuous drain current of 5.1A, and a pulse drain current of 35A (2001b). The diameter of the solder joint in this module is $250\mu m$. The drain current is carried by two solder joints so that each solder joint is carrying 2.55A continuous current. This leads to a current density of $0.52\times10^4 A/cm^2$ in each solder joint. The pulse drain current density in either of these two solder joints is as high as $3.6\times10^4 A/cm^2$.

Another commercial example is the FDZ203N PowerTrench® BGA MOSFET from Fairchild Semiconductor Corporation (Figure 5b). This power module is designed to

handle 20V drain-source voltage, 7.5A continuous drain current, and 20 A pulse drain current. The size of this module is only $5mm^2$ with a low profile of 0.7mm in height. Three solder joints are used to carry the drain current with a diameter of 300μm. Each solder joint is design to carry 2.5A of continuous drain current or a current density of $0.354\times10^4 A/cm^2$. The pulse drain current will cause a current density of $0.94\times10^4 A/cm^2$. These two examples show that the current density in solder joints of present day flip-chip packaged power modules is near 10^4A/cm2. The current density in solder joints of flip-chip packaged power modules will be much higher if they are designed to handle more current or further reduce their size.

The current density in solder joints of microelectronic packaging is much lower than that in flip-chip power packaging. But this may change as the continuous miniaturization trend of IC devices for cost reduction, increased functionality, and portability. The solder joints are expected to satisfy the future need of high on-chip I/O connections and to achieve a uniform distribution of voltage drop across the entire chip surface (Tang and Shi 2001). This leads to a smaller solder joint size which causes very high current densities within the solder joint. As predicted in the National Technology Roadmap for Semiconductors (1997), the number of solder joints needed on a 1×1 cm^2 IC chip can be up to 10,000. This means the diameter and pitch of the solder joints need to be reduced to 50μm and 100μm, respectively. Current circuit design rules require that each interconnect carry a current of up to 0.2 Amp, with an increase to 0.4 Amp in the near future. A current of 0.2 Amp through a solder joint of 50μm in diameter results in a current density of $1x10^4$ Amp/cm^2. Therefore, the reliability of solder joint under high

electrical stressing is essential for both high power electronic packaging and microelectronic packaging.

Although this current density is lower that that found in Al or Cu traces in semiconductors, the solder has a low melting point and, therefore, greater atomic diffusivity at higher operating temperature (Lee et al. 2001a). Under this high current stressing, a diffusion process occurs that causes metal atoms to drift in the direction of the electron flow. The diffusion of solder alloy atoms causes microvoids to form along the cathode end and pileup or hillocks along the anode end. The voids decrease the cross-sectional area of the solder joint and increase the local current density and local resistance. This expected positive feedback cycle may eventually lead to a so-called electromigration-induced catastrophic failure (Tang and Shi 2001). Published works report the observation of electromigration of solder joints and solder strips (Brandenburg and Yeh 1998;Liu et al. 1999a;Hu and Harper 1998;Lee et al. 2001a).

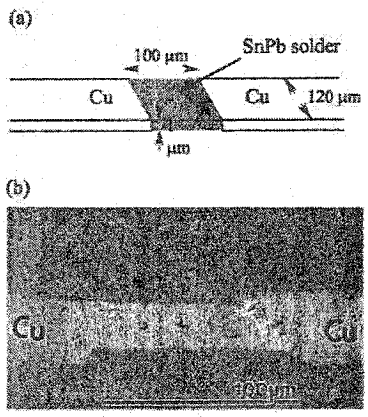


Figure 6 (a) Schematic picture of the eutectic SnPb solder thin strip sample. (b) the SEM image of an eutectic SnPb solder strip stressed by a direct electrical current of 105 amp/cm2 at room temperature for 19 days. (after Liu (Liu et al. 1999a))

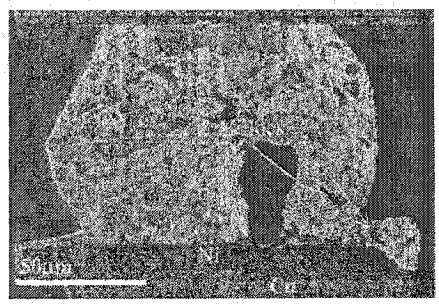


Figure 7 SEM micrograph of the solder ball after 324 h current stressing (after Lee (Lee et al. 2001a))

In an experiment conducted by Liu et al. (Liu et al. 1999a), room temperature electromigration was observed in a eutectic SnPb solder strip stressed by a current density of 10^5 Amp/cm^2. Hillocks grow at the anode and voids grow at the cathode as shown in Figure 6. Sn is the dominant diffusion species in the solder alloy. Lee et al. studied the electromigration of eutectic SnPb solder interconnects between a Si chip and a FR4 substrate at 120°C for up to 324 hours with a current stressing of 10^4 Amp/cm^2 (Lee et al. 2001a). Hillocks were observed at the anode and voids at the cathode (Figure 7). The dominant diffusing species was Pb, which is confirmed by its accumulation at the anode. The difference in dominant diffusion species in these two experiments is mainly because the diffusion paths in the alloy are different at room temperature than at elevated temperature. Liu et al. (Liu et al. 2000a) reported on the electromigration in Sn-Pb solder strips for different alloy compositions. The eutectic alloy, with the lowest melting point and a high density of lamella interfaces, was found to have the fastest hillock growth.

1.3 Goals

After the reviewing the reliability issues in power electronic packaging, the research in this dissertation is focused on the mechanical reliability of solder joints under

electrical stressing. The flip-chip technique is the packaging technique for next generation high speed, high performance power modules (Liu et al. 2000b;Liu et al. 1999b;Liu and Lu 2001). By removing wire bonding interconnects, the BGA packaging technique eliminates the frequently occurring failures in wire bonding power modules (wire bonding lift-off and heal-cracking), and provides better electrical performance. The reliability of solder joint becomes essential for the reliability of next generation power modules. The solder joint in a BGA power module is subjected to thermal, mechanical and electrical stressing in its working condition. There has been extensive researches on the reliability of BGA packaging under thermomechanical stressing reported in the literature (Basaran and Yan 1998;Basaran and Chandaroy 1998;Chandaroy 1998;Dasgupta et al. 1992;Desai et al. 1997;Ju et al. 1994;Knecht and Fox 1990;Lau et al. 1996;Ozmat 1990;Pitarresi and Akanda 1993;Qian et al. 1999). However, the electrical current density in power module is so high that it cannot be ignored as a reliability concern. The main trust of this dissertation is focused on the mechanical reliability of solder joints under electrical stressing. The mechanical reliability of solder joints under high density current stressing has never been studied in a formal research project. An extensive literature survey on the subject indicates that there is a big vacuum in this field. This work attempts to fill that vacuum.

The goals of this dissertation can be summarized as follows:

1.1 To measure the displacement evolution in a BGA solder joints under high current stressing with the Moiré Interferometry technique.

1.2 To develop a material constitutive model for solder alloy under current stressing.

1.3 To provide a basic understanding of the failure mechanism and damage process of solder joints under high density current stressing.

1.4 Outline

The rest of this dissertation is organized as follows. Chapter 2 contains a detailed literature survey, on the physics of electromigration, experimental and theoretical research of electromigration in thin metallic film, as well as latest experimental research of electromigration in solder joints. In Chapter 3, a partial differential equation system of electromigration modeling is presented and implemented with finite element analysis. Chapter 4 presents the measurement of the displacement evolution of BGA solder joints under current stressing and their numerical simulation. Chapter 5 reports failure modes and microstructural evolution of flip-chip solder joints under current stressing. Chapter 6 proposes several avenues for future work.

Chapter 2

Literature Survey

2.1 Physics of Electromigration

Electromigration is a mass diffusion-controlled phenomenon. When a conductor solid is subject to a high current density, the so-called electron-wind transfers part of the momentum to the atoms (or ions) of solid to make the atoms (or ions) move in the direction of the electron flow. It was first identified as a reliability problem in the integrated circuit more than 30 years ago (Blech and Sello 1965;Blech and Sello 1966). But the phenomenon of electromigration and its basic physics was studied 50 years ago (Schwarz 1945;Seith 1955;Jost 1952). The work of Fiks (Fiks 1959;Fiks 1964) and Huntington (Huntington and Grone 1961) some 40 years ago has been the basis for the understand of electromigration, and it has been improved upon in subsequent years (Sorbello 1973;Bosvieux and Friedel 1962;Das and Peierls 1973;Landauer 1975;Schaich 1976;Lodder and Brand 1984;Chu and Sorbello 1991).

2.1.1 Electromigration Physics

In the early 1950s, Seith and Wever used the surface markers technique in the study of various Hume-Rothery alloys as a function of composition and revealed a direct correlation between the sign of the charge carriers and the direction of net mass motion (Seith and Wever 1953;Wever and Seith 1955). They considered the possible effect of momentum exchange between the charge carriers and the moving atoms (or ions; the

terms "atom" and "ion" are used interchangeably) based on this observation. This possibility was originally suggested by Skaupy (Skaupy 1914) in 1914 who introduced the concept of "electron wind" as a driving force in the process of electromigration. Such an electron wind force drives positive ions in the direction of electron flow, which is opposite to the direction of the electrostatic force of the electric field. Figure 8 shows the schematic of electron wind force (due to the momentum exchange from collisions between conducting electrons and diffusion metal atoms) and direct electrostatic force exerted on the atoms in a metal conductor.

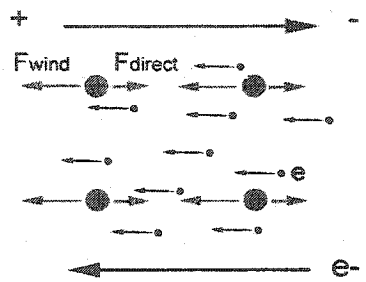


Figure 8 Kinematics of electromigration process

Therefore, the driving force exerted on an ion is then (Huntington 1972)

$$\vec{F} = \vec{F}_{wind} + \vec{F}_{direct} = (Z_{wind} + Z_{el})e\vec{E} = Z^* e\vec{E} = Z^* e\rho\vec{j} \qquad (2.1)$$

where Z_{wind} is the valence number arises from the electron wind force, Z_{el} is the nominal valence of an ion, Z^* is called effective valance (or effective charge number), which is combined from the electron wind force and electrostatic force, e is electron charge, $\vec{E}$ is the macroscopic electric field, which is related to the electric potential ψ according to $\vec{E} = -\vec{\nabla}\psi$, ρ is resistivity, and $\vec{j}$ is current density. Z^* is commonly negative in metal conductors because of the influence of the "electron wind."

There are various theoretical approaches for the calculations of Z^* (see Sorbello (Sorbello 1991) for a complete review), among them the ballistic model is the most

widely used. The ballistic model for electromigration driving force was independently developed by Fiks (Fiks 1959) and Huntington (Huntington and Grone 1961), and it emphasizes the actual collisions between the current carrying charges and the moving atoms of the lattice. Fiks treats the number of collisions of the ions with the charge carriers (free electrons or holes) per unit time as equal to the product of $nv\sigma_{tr}$, where n is the density of the charge carriers, v is the average velocity, and σ_{tr} is the intrinsic cross-section for collision between the carriers and the moving ions. For each collision, the carrier transfers on the average the momentum that is picked up from the field during one relaxation time τ (life time of the activated state for an ion), or $-e\vec{E}\tau$ (if electron is the charge carrier). The momentum change per unit time, or the electron wind force:

$$\vec{F}_{wind} = -e\vec{E}\tau \cdot nv\sigma_{tr} \tag{2.2}$$

Let $l=v\tau$ (called electron mean-free-path), Equation (2.2) can be rewritten as

$$\vec{F}_{wind} = -en\vec{E} \cdot l\sigma_{tr} \tag{2.3}$$

thus $$Z_{wind} = -nl\sigma_{tr} \tag{2.4}$$

and $$Z^* = Z_{el} - nl\sigma_{tr} \tag{2.5}$$

From Equation (2.5), it is easy to understand why for simple metals the electron wind force dominates the direct force and therefore Z^* is negative. This is because $nl\sigma_{tr}$, which is the number of electrons contained in a fictitious cylinder of length l and cross-section σ_{tr}, is much larger than Z_{el} (Sorbello 1991).

The Huntington and Grone's postulation (Huntington and Grone 1961) is a little bit different from Fiks'. Their treatment postulates a transition probability between free

electron states induced by scattering from the moving ions. It is demonstrated that their postulation gives equivalent results to Fiks' (Huntington 1972).

Besides the ballistic model, there are other alternatives to treat electron wind driving force. Bosvieux and Friedel (Bosvieux and Friedel 1962) postulated the polarization charge model, in which they calculated the force exerted on an ion from the polarization of the electrons in the applied field. In their approach, the collision concept is not explicitly mentioned but the nature of the defect shielding by the free electron charge is explored. They also considered the force exerted by the asymmetric distribution in the neighborhood of a vacancy on a marked atom at a next neighbor site. They found it to be small, but not negligible and quite dependent on the structure of the matrix of atoms. This particular result illustrates one of the advantages of this method over the ballistic model, which always left rather unresolved the question of how the scattered momentum of the charge carriers was to be distributed between the moving ion and its immediate neighbors (Huntington 1972). The prime virtue of the Bosvieux and Friedel approach is that it can be generalized to systems more complicated than an isolated ion in a free electron gas (Sorbello 1991). Based on the polarization charge model, Kumar and Sorbello (Kumar and Sorbello 1975) introduced Kubo linear-response formalism into electromigration. In so doing, they cast the electromigration problem into a rigorous framework which allowed many-body techniques to be used (Sorbello 1991). The formulation (Sorbello 1985) based on this theory showed that the direct electrostatic field force valence Z_d is neither zero (the Bosvieux-Friedel value) nor Z_{el} (the Huntington-Fiks value), but instead was typically on the order of 10%-30% smaller than Z_{el}.

Now let us discuss the diffusion equation in metals with an electromigration driving force. Huntington (Huntington 1975b;Huntington 1975a) demonstrated that the atomic flux J_a of the mobile ions by the driving force $\vec{F}$ can be expressed by the Nernst-Einstein equation:

$$J_a = -D_a \vec{\nabla} C_a + \frac{D_a C_a}{kT} \vec{F} \tag{2.6}$$

where D_a is the atomic diffusivity, C_a is the atomic concentration, k is Boltzman's constant, and T is absolute temperature. If only electromigration driving force is considered as expressed in Equation (2.1), the atomic flux due to electromigration is expressed as:

$$J_a = -D_a \vec{\nabla} C_a + \frac{D_a C_a}{kT} Z^* e \vec{E}$$

or

$$J_a = -D_a \vec{\nabla} C_a + \frac{D_a C_a}{kT} Z^* e \rho \vec{j} \tag{2.7}$$

where ρ is resistivity, and $\vec{j}$ is current density, since $\vec{E} = \rho \vec{j}$.

2.1.2 Thermodynamic Formulation

Let us consider the response of electrons and ions in the metal to an applied electric field. According to generalized thermodynamic coupling theory for the near-equilibrium case (a system near equilibrium is one in which the driving forces are all small), one can expand the fluxes in terms of small driving forces (Carter and Allen 2002). For simplicity, only one atomic species is assumed in system. If the electron flux is denoted by $\vec{J}_e$ and the atomic flux is denoted by $\vec{J}_a$, the coupling force-flux relationship at constant temperature is given by Hungtington (Huntington 1975b):

$$\vec{J}_a = -L_{aa}\vec{\nabla}(\mu_a + Z_{el}e\psi) - L_{ae}\vec{\nabla}(\mu_e - e\psi)$$
$$\vec{J}_e = -L_{ea}\vec{\nabla}(\mu_a + Z_{el}e\psi) - L_{ee}\vec{\nabla}(\mu_e - e\psi) \quad (2.8)$$

where μ_a and μ_e are the chemical potentials of the ions and electrons, respectively, e is electron charge, Z_{el} is the nominal valence of the ion, ψ is electrical potential, and coefficients L_{aa}, L_{ae}, L_{ea} and L_{ee} are the linear coefficients of driving forces around the equilibrium state (i.e. the case of condition of small driving forces), similar to spring coefficients in a 2- DOF (Degree of Freedom) system. The coupling between electron and ion fluxes is described by the cross terms L_{ae} and L_{ea}. According to Onsager's Symmetry Relationship, $L_{ae} = L_{ea}$. There is usually no electron concentration gradient in the conductor ($\vec{\nabla}\mu_e = 0$). The first equation in Equation (2.8) is thus:

$$\vec{J}_a = -L_{aa}[\vec{\nabla}\mu_a + (Z_{el} - \frac{L_{ae}}{L_{aa}})e\vec{\nabla}\psi] \quad (2.9)$$

Chemical potential of a thermodynamic system is the change in the free energy of the system when an additional constituent particle is introduced. The chemical potential of ions can be related to local concentration through the activity coefficient γ_a (Carter and Allen 2002):

$$\mu_a = \mu_0 + kT \ln \gamma_a C_a \quad (2.10)$$

where μ_0 is the chemical potential of ions at reference state, k is Boltzman's constant, and T is absolute temperature. For the ideal case, the activity coefficient is independent of concentration, so

$$\vec{\nabla}\mu_a = \frac{kT}{C_a}\vec{\nabla}C_a$$

The Onsager coefficient L_{aa} is derived to be $\frac{D_a C_a}{kT}$ following a kinetic formulation (Carter and Allen 2002). Let $\vec{E} = -\vec{\nabla}\psi$, which is the electric field, Equation (2.9) becomes:

$$\vec{J}_a = -D_a \vec{\nabla} C_a + \frac{D_a C_a}{kT}(Z_{el} - \frac{L_{ae}}{L_{aa}})e\vec{E} \qquad (2.11)$$

If we let $Z^* = Z_{el} - L_{ae}/L_{aa}$ be the effective charge number, Equation (2.11) becomes identical to Equation (2.7), which is derived from the electromigration physics formulation. The fact that Z^* for metals is usually negative and large in magnitude indicates that the kinetic coupling described by $-L_{ae}/L_{aa}$ term is usually dominant (Sorbello 1991).

2.2 Research on Electromigration in Thin Metal Films

The phenomenon of electromigration was observed more than half a century ago and attracted lots of academic curiosity (Schwarz 1945;Seith 1955;Jost 1952;Fiks 1959;Fiks 1964;Huntington and Grone 1961). It was not until 30 years ago, when electromigration was identified as failure mechanism responsible for open-circuit failure in the integrated circuit (Blech and Sello 1965;Blech and Sello 1966;Blech and Sello 1967;Chhabra and Ainslie 1967), that it become the subject of intensive research and development. The thin metal films employed in microelectronic devices carry very high current density due to their extremely small size. The current density in these thin films is near or in excess of $10^6 A/cm^2$ (Lloyd 1999b). At such high current density, electromigration can become significant. Electromigration has become one of the

principal limiting factors in achieving higher performance microprocessors (Lloyd 1999b).

2.2.1 Electromigration and Stress

James R. Black (Black 1967) was one of the pioneers in conducting research on the failure mechanisms of electromigration in thin metal conductors. He found that the lifetime of a thin metal conductor is inversely proportional to the square of the current density and has an Arrhenius component with an activation energy consistent with grain boundary diffusion. He proposed the following median time to failure equation:

$$t_{50} = \frac{A}{j^n} \exp\left(\frac{E_a}{kT}\right) \tag{2.12}$$

where t_{50}, median time to failure (MTTF), is defined as the time at which 50% of a large number of identical devices have failed, A is a empirical material constant, j is the current density, n is the current density exponent and is found to be 2 in Black's experiments, E_a is the activation energy, k is Boltzman's constant, and T is the absolute temperature. This equation is known as Black's Equation. The n = 2 behavior in Black's experiment is intuitively contradictory to Equation (2.1), where the electromigration driving force is linearly proportional to current density. From Equation (2.1), one might conclude that electromigration failure time would be inversely proportional to the current density. This discrepancy has motivated many researches to try to explain it. In his electromigration experiments on Aluminum film with different grain sizes, Black (Black 1969) found that large-grained film had a higher activation energy and yielded significantly longer lifetime than finer-grained films. He attributed these increases to the reduction of grain

boundaries with their associated high diffusivity. He also found that Al films with a tough overcoat had higher activation energy and a longer lifetime (Black 1969).

In order to explain the discrepancy between $n = 2$ behavior from Black's experiment and the theoretical understanding described in Equation (2.1), early analytical models of electromigration failure considered that the diffusion equation contained a concentration gradient term ((Rosenberg and Ohring 1971;Shatzkes and Lloyd 1986)):

$$\frac{\partial C}{\partial t} = \frac{\partial J}{\partial x} = D\left(\frac{\partial^2 C}{\partial x^2} - \frac{Z^* e \rho j}{kt}\frac{\partial C}{\partial x}\right) \tag{2.13}$$

where C is vacancy concentration and J is vacancy flux. By solving the above equation for the boundary conditions $J(0,t) = 0$ (blocking boundary) and $J(-\infty,t) = C_0$, they found that the time to achieve a specific concentration level is proportional to the inverse square of the current density (Shatzkes and Lloyd 1986):

$$t_f = B\frac{T^2}{j^2}\exp\left(\frac{E_a}{kT}\right) \tag{2.14}$$

This solution has the same current dependence as Black's equation, but different temperature dependence. Clement and Lloyd numerically solved Equation (2.13) with different boundary conditions (Clement and Lloyd 1992). They found that regardless of the boundary condition chosen, the time to achieve certain concentration level approximates the semi-infinite solution of Shatzkes and Lloyd (Shatzkes and Lloyd 1986) as long as the critical concentration is away from the steady state value (Clement and Lloyd 1992). However, these models do not include the effect of stress on electromigration. Additionally, when reasonable values for parameters were inserted into Equation (2.14), the life time predictions obtained were too short (Lloyd 1999a).

Black attributed the increase in lifetime for those films with silica glass coating to the reduction in surface diffusion (Black 1969). Other researchers also found positive effects of an overlying passivation layer on the electromigration lifetime of thin films (Spitzer and Schwartz 1969;Blair 1970). In 1972, Ainslie et al (Ainslie et al. 1972) first recognized that mechanical stress may play an important role in electromigration damage. They suggested that a stress gradient may oppose electromigration flow and the stress may affect the diffusivity. But they underestimated the possible stress level that can be obtained in thin film during electromigration. The importance of stress to electromigration was first demonstrated in experiments by Blech (Blech 1976;Blech and Herring 1976;Blech and Tai 1977;Blech and Kinsbron 1975). In a series of "drift" experiments, thin metal films were deposited onto a high-resistance, refractory substrate. Electric current was applied and the edge of the film closer to the cathode was observed to move towards the anode with a certain drift velocity. It was discovered that the drift velocity was a function of the film length. Longer film showed a much higher drift velocity than short ones. He found that a threshold or critical film length exists for electromigration, under this length no electromigration edge drift will occur (Figure 9).

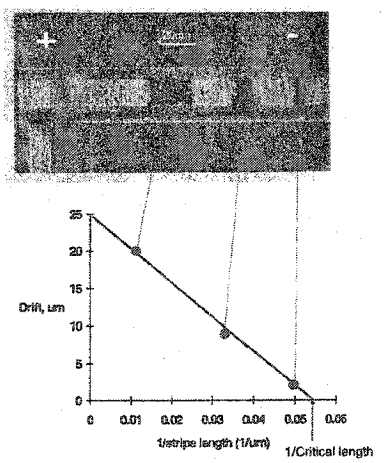


Figure 9 Drift of four aluminum strips with varying lengths (heat treated 350°C, 20h) after passage of 3.7×10^5A/cm^2 (after Blech (Blech 1976))

This critical length was found to be inversely proportional to current density (Blech 1976). The experiments suggested that ions transported by the electromigration create a stress and/or concentration differences between the film ends causing a back flow that counteracts the electromigration. Under critical length, a back flow created by pressure gradients balances the forward electromigration flow, thus eliminating any net flow (Blech and Herring 1976):

$$Z^* e \rho j = \Omega \frac{\partial \sigma_{nn}}{\partial x} \tag{2.15}$$

Where Ω is the atomic volume, σ_{nn} is the stress normal to the grain boundaries, Z^*, e, ρ, j have the usual meaning. The critical length can be calculated from Equation (2.15) if the maximum stress that can be sustained in the thin film until failure is given. This is usually expressed as the "Blech product":

$$jl_{Blech} = \frac{(\sigma_{\max} - \sigma_0)\Omega}{Z^* e \rho} \tag{2.16}$$

where σ_{max} is the maximum stress that can be supported by the metal film before failure and σ_0 is the stress at the other end of the film (Blech 1998). With an in-situ observation experiment by transmission X-ray topography, Blech and Herring confirmed the stress gradient build-up in thin Al films during passage of electrical current (Blech and Herring 1976;Blech and Tai 1977).

2.2.2 Stress Evolution during Electromigration in Thin Metal Lines

Equation (2.15) gives only the steady state distribution of stress in the thin metal line under current stressing, but gives no information about how the stress builds up. Ross (Ross 1991) and Kirchheim (Kirchheim 1992) were the first to model the transient stress

evolution during electromigration. Ross' model is essentially numerical, while Kirchheim proposes a physically-based model involving two coupled differential equations (Korhonen et al. 1993).

In Kirchheim's approach, electromigration is described as a biased diffusion of vacancies. The vacancy flux and atomic flux must be the same in a vacancy controlled diffusion mechanism (Lloyd 1995). But the difference is that vacancy has a limited lifetime while atoms can not be generated or annihilated. The vacancy diffusion equation of Shatzkes and Lloyd and subsequent papers (Shatzkes and Lloyd 1986;Clement and Lloyd 1992) were flawed in the sense that a supersaturation of vacancies cannot be supported in a thin film as described (Lloyd 1999a). The thermal equilibrium vacancy concentration at a stress-free state is given by $C_{v0} = C_L \exp(-E_a^v / kT)$, where E_a^v is the activation energy for vacancy formation in the location of interest (lattice, grain boundary, or interface) and C_L is lattice concentration (Lloyd 1995). The thermal equilibrium vacancy concentration will increase in the presence of mechanical stress, and is given by Kirchheim as $C_{ve} = C_{v0} \exp(f'\Omega\sigma / kT)$, where $f' = 1 - f$ (f is the vacancy relaxation ratio), Ω is atomic volume, σ is mechanical stress. It is proposed that vacancy will generate or annihilate in grain boundaries if their concentration deviates from the equilibrium value. This is considered by adding a source term, $(C_v - C_{ve})/\tau_s$, to the vacancy continuity equation:

$$\frac{\partial C_v}{\partial t} = -\frac{\partial J_v}{\partial x} - \frac{C_v - C_{ve}}{\tau_s} \qquad (2.17)$$

where C_v vacancy concentration , J_v is vacancy flux, τ_s is characteristic generation/ annihilation time. The vacancy flux is considered to be the combination of flux due to

concentration gradient, electrical field forces, and stress gradient in Kirchheim's formulation:

$$J_v = -D_v \frac{\partial C_v}{\partial x} + \frac{D_v C_v}{kT} Z^* e \rho j - \frac{D_v C_v}{kT} f \Omega \frac{\partial \sigma}{\partial x} \tag{2.18}$$

where Z^*e is effective charge, j is current, D_v is vacancy diffusivity, f is vacancy relaxation ratio (ratio of a volume of a vacancy to volume of an atom), Ω is atomic volume. A direct relationship between the rate of change of stress and the action of the vacancy source term is proposed as:

$$\frac{\partial \sigma}{\partial t} = Bf' \Omega \frac{\delta}{d} \frac{C_v - C_{ve}}{\tau_s} \tag{2.19}$$

where B is the bulk modulus, $f' = 1 - f$, δ is grain boundary thickness, and d is grain size. By solving the coupled differential equations (2.18) and (2.19), we can find both the vacancy concentration evolution and transient stress build-up in the thin film conductor. Kirchheim found that the mechanism for concentration change with the smallest characteristic length in a given problem determines the concentration profile at a quasi-steady state (Kirchheim 1992).

Korhonen et al (Korhonen et al. 1993) also suggested that vacancies would annihilate/generate at convenient sites and therefore produce stress in the thin metal line covered by a rigid dielectric passivation layer. They assume that the material transport along the interconnect line is affected by grain boundary diffusion alone. When a net number of atoms entering a local volume of the interconnect line (either they can be spent in changing the vacancy concentration or be deposited on grain boundaries or lattice dislocations), the deposition of atoms creates lateral stresses σ_1 and σ_2 because of the confinement by the surrounding rigid dielectric (Korhonen et al. 1993) as well as σ_3 due

to the Poisson effect. They assume that in thermal equilibrium, the chemical potential in any cross section is constant at all grain boundaries, such that the arising lateral stresses across the boundaries is equal, i.e., $\sigma = \sigma_1 = \sigma_2$. Therefore, in this particular model, only one stress component is addressed. Using the Eshelby elastic theory of inclusion (Eshelby 1957), the stresses created by deposition of atoms at grain boundaries is derived as (Korhonen et al. 1993):

$$\frac{dC_L}{C_L} = -\frac{d\sigma}{B} \tag{2.20}$$

where C_L is the lattice concentration (the number of available lattice site per unit volume), B is the applicable modulus (depends on the elastic properties of metal line and passivation layer, and on the aspect ratio of line thickness and width). The lattice concentration is related to atomic concentration and vacancy concentration by: $C_L = C_a + C_v$. The diffusion continuity equation is thus:

$$-\frac{\partial J_a}{\partial x} = \frac{\partial C_v}{\partial t} + \left(\frac{C_L}{B}\right)\frac{\partial \sigma}{\partial t} \tag{2.21}$$

where J_a is the atomic flux and expressed by Korhonen as:

$$J_a = -\frac{D_a C_a}{kT}(\nabla \mu + Eq^*) \tag{2.22}$$

where D_a is atomic diffusivity, $\mu = \mu_0 - \Omega\sigma$ (Herring 1971;Herring 1950), is the chemical potential, q^* is the effective charge, Ω is atomic volume, and E is electric field. In Korhonen et al model, the vacancies are assumed to be in equilibrium with stress (such that $\mu_v = 0$, where μ_v is vacancy chemical potential) all the time:

$$C_v = C_{v0} \exp[(W_f + \Omega\sigma)/kT] \tag{2.23}$$

where C_{v0} is the vacancy concentration in the absence of stress, and W_f is the interaction energy between the vacancy and the stress field (Balluffi and Granato 1979). In this model, W_f is assumed to be zero. By further approximating that $C_L = C_a = 1/\Omega$ and $(C_v / C_L)B\Omega / kT \ll 1$, a one dimensional expression of stress evolution along the metal line during electromigration is derived as (Korhonen et al. 1993):

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}[\frac{D_a B\Omega}{kT}(\frac{\partial \sigma}{\partial x} + \frac{Eq^*}{\Omega})] \tag{2.24}$$

This model presents a good understanding of the origin of the stress in the thin metal line due to electromigration and gained wide acceptance. By assuming the stress to reach a critical level (i.e., yield stress) as the failure criteria, the solution of Equation (2.24) for blocking diffusion boundaries gives power of -2 dependence of failure time to current density, which agrees with Black's experiments.

Clement and Thompson (Clement and Thompson 1995) re-examined the assumptions and approximations in the Korhonen treatment, and reformulated an analytic expression for the evolution of the stress in confined interconnect lines. In their approach, electromigration is described as a vacancy diffusion equation with a sink/source term:

$$\frac{\partial C_v}{\partial t} + \frac{\partial J_v}{\partial x} + \gamma = 0 \tag{2.25}$$

where J_v is the vacancy flux and γ is the vacancy generation/annihilation rate. They expressed the sink/source term as:

$$\gamma = -\frac{\partial C_L}{\partial t} \tag{2.26}$$

Clement and Thompson used the same assumption as the Korhonen model that the vacancies are in equilibrium with stress and followed the stress-lattice concentration

relationship developed in Korhonen model (Equation (2.20)). Their stress evolution equation is derived as:

$$\frac{\partial \sigma}{\partial t} = \frac{B}{C_L}\frac{\partial}{\partial x}[\frac{C_v D_v \Omega}{kT}(\frac{\partial \sigma}{\partial x} + \frac{q^* E}{kT})] \tag{2.27}$$

The difference between this derivation and Korhonen model is that the approximation $C_L = C_a = 1/\Omega$ is not taken. If this approximation is taken, Equation (2.27) can be reduced to the Korhonen model (Equation (2.24)) by using the relationship between vacancy diffusivity and atomic diffusivity, $D_a C_L = D_v C_v$. They argued that Korhonen model is a good approximation under the condition that the maximum stress is relatively small and their formulation is more accurate (Clement and Thompson 1995). This model is later improved by Clement (Clement 1997) with the consideration of a ratio of the line cross sectional area to the area of the diffusion path, ε, in the vacancy sink/source term:

$$\gamma = -\varepsilon \frac{\partial C_L}{\partial t} \tag{2.28}$$

2.2.3 More General Models of Stress Evolution due to Electromigration

One of the common characteristics of aforementioned stress evolution models is that they all use a direct relationship between the stress (often just one component) and some kind of concentration change (lattice or vacancy concentration). Korhonen justified the usage of only one stress component by arguing that atoms are deposited at differently oriented grain boundaries such that the lateral normal stresses across the boundaries become equal in thermal equilibrium (Korhonen et al. 1993). The direct relationships between the stress and concentration are derived from the assumption that the metal line has elastic material properties and is limited to a particular geometry and boundary

condition (one dimensional line confined in the passivation layer). Therefore, it is clear that these models cannot be extended to the more general case of electromigration in which either material is highly inelastic or the conductor has different geometry and boundary conditions. For example, they cannot be used to model electromigration of a solder joint, which is spherical in shape and highly viscoplastic in material properties. In order to model the electromigration of a solder joint, these material and geometry assumptions have to be abandoned.

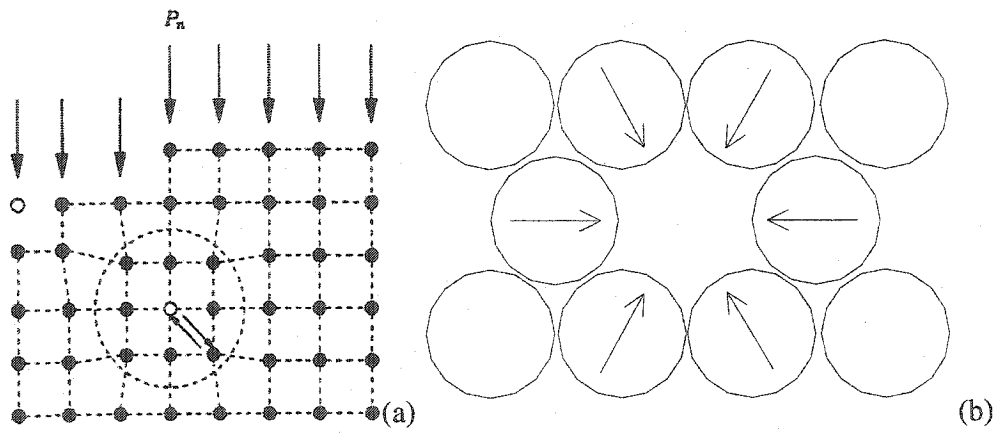


Figure 10 (a) Lattice showing local volumetric strain (indicated by the dashed circle) due to relaxation of atoms around a vacancy and normal traction Pn acting on free surface. Atoms are represented by filled circles and vacancies by open circles. Vacancies are able to switch lattice sites with adjacent atoms (after Bassman (Bassman 1999)). (b) Larger schematic of local volumetric deformation due to vacancy migration

Bassman and Garikipati (Bassman 1999;Garikipati et al. 2001) proposed general micromechanical continuum formulation for stress-driven mass diffusion in polycrystalline solids. In this treatment, electromigration is just one of the driving forces for diffusion. The same assumption as Kirchheim (Kirchheim 1992) is used: the vacancies will generate or annihilate in grain boundaries if their concentration deviate from the equilibrium value. This is reflected by a source term in the vacancy continuity equation

$$\frac{\partial C_v}{\partial t} = -\vec{\nabla} \cdot \vec{J}_v - \frac{1}{\tau}(C_v - C_v^{eq})\chi \tag{2.29}$$

where J_v is vacancy flux, τ is a time constant that defines the effectiveness of vacancy source/sink, C_v^{eq} is the thermal equilibrium vacancy concentration in the presence of stress, and χ is an indicator function which designates grain boundary ($\chi = 1$) and lattice ($\chi = 0$). The vacancy generation/annihilation is explicitly restricted in grain boundary as indicated by χ. In this formula, the vacancy diffusion is related to the deformation in the solid (Figure 10) and no immediate relationship with stress is assumed. The complete elastic strain is (Bassman 1999):

$$\varepsilon^e = \varepsilon - \theta_T \mathbf{1} - \frac{1}{3}\theta_a \mathbf{N} + \theta_v \mathbf{1} \tag{2.30}$$

where $\theta_T = 3\alpha_T \Delta T$ is the thermal strain, θ_v is vacancy relaxation strain, θ_a is called creep strain, and $\mathbf{N} = \mathbf{n} \otimes \mathbf{n}$ ($\mathbf{n}$ is the unit vector perpendicular to the grain boundary). θ_v and θ_a are due to diffusion and are superimposed on thermomechanical strain tensor. They proposed that a vacancy concentration C_v causes a vacancy relaxation strain θ_v relative to the reference state:

$$\theta_v = (1 - f)\Omega_a (C_v - C_{v0}^{eq}) \tag{2.31}$$

where f represents the fractional volume of a vacancy relative to an atom volume, Ω_a is atomic volume, C_{v0}^{eq} is thermal equilibrium vacancy concentration in the stress-free lattice. In simple terms vacancy relaxation strain is imposed when a vacancy switches lattice site with an atom. The creep strain is defined as:

$$\theta_a(x,t) = \Omega_a \int_0 [-\frac{1}{\tau}(C_v - C_v^{eq})] ds \tag{2.32}$$

This creep strain accounts for the strain due to atoms deposited in grain boundaries; however, θ_a may be considered to be only in the direction of the normal to a boundary. The stress tensor is determined from the mechanical equilibrium equation with appropriate mechanical constitutive model being applied. Although an elastic constitutive model is used in this work, an inelastic mechanical model can also be applied with this approach. Because stress is one of the driving forces for vacancy diffusion, the stress evolution can only be found by solving the coupled diffusion and mechanical equilibrium equations. Bassman (Bassman 1999) showed the effectiveness of this model in simulating single grain Nabarro-Herring creep, Coble creep, and multigrain electromigration. Since the grain boundaries and lattice are treated explicitly in this model, the detailed grain structure is needed in the analysis and therefore too complicated for analysis of a real structure.

Using similar concept, Sarychev (Sarychev and Zhinikov 1999) proposed that the vacancy diffusion causes volumetric strain in the metal during current stressing. This volumetric strain is composed of two parts, ε_{ij}^m, the volumetric strain due to vacancy flux divergence, and ε_{ij}^g, the volumetric strain due to vacancy generation. Since diffusion is a time dependent process, these volumetric strains are naturally expressed in the form of strain rates,

$$\dot{\varepsilon}_{ij}^m = \frac{1}{3} f \Omega \vec{\nabla} \cdot \vec{J}_v \delta_{ij} \tag{2.33}$$

$$\dot{\varepsilon}_{ij}^g = \frac{1}{3}(1-f)\Omega G \delta_{ij} \tag{2.34}$$

where f is vacancy relaxation ratio, Ω is atomic volume, J_v is vacancy flux, G is vacancy generation rate, δ_{ij} is the Kronecker's symbol. Thus, the combined volumetric strain rate due to current stressing is:

$$\dot{\varepsilon}_{ij}^{elec} = \dot{\varepsilon}_{ij}^{m} + \dot{\varepsilon}_{ij}^{g} = \frac{\Omega}{3}[f\vec{\nabla}\cdot\vec{J}_v + (1-f)G]\delta_{ij} \tag{2.35}$$

The total volumetric strain rate due to current stressing is then:

$$\dot{\varepsilon}^{elec} = \Omega[f\vec{\nabla}\cdot\vec{J}_v + (1-f)G] \tag{2.36}$$

By analogy to thermal strain (which is the volumetric strain caused by temperature variation), the volumetric strain caused by the current stressing is superimposed onto the strains tensor with strains due to other loadings. The total strain can be given by:

$$\varepsilon_{ij}^{total} = \varepsilon_{ij}^{mech} + \varepsilon_{ij}^{therm} + \varepsilon_{ij}^{elec} \tag{2.37}$$

where ε_{ij}^{total} is the total strain tensor, ε_{ij}^{mech} is the strain due to mechanical loading, ε_{ij}^{therm} is the strain due to thermal load, and ε_{ij}^{elec} is the volumetric strain due to electromigration. In Sarychev's proposed model, the vacancy diffusion equations are taken from Kirchheim, in which a vacancy sink/source term is included in the vacancy continuity equation. The stress fields are calculated as a result of volumetric strain induced by electromigration. In this approach, the assumptions of elastic material properties, particular geometry, and boundary conditions are no longer necessary. All the components of a stress tensor, not just spherical stress, are available by solving the coupled diffusion and mechanical equilibrium equations.

2.2.4 Other Developments on Stress Evolution in Thin Films due to Electromigration

Trattle, et al. (Trattles et al. 1994) developed a model in which the back-fluxes are explicitly calculated in each of the grain boundaries using concentration and stress gradients that result from the initial electromigration flux. This work considers stress-dependent atomic diffusivity. It was assumed in the model that the main cause of flux divergence is the grain structure of the metal line and the divergences occur at the triple-point junctions of the grain boundary. Detailed grain structure of the metal line is considered in the simulation. In the work proposed by Gleixner and Nix (Gleixner and Nix 1999), the detailed grain structure of the thin metal film was also considered. The electromigration is expressed by an atomic diffusion equation, in which different diffusion paths, including lattice, grain boundaries, and surrounding interfaces, are treated individually. The gradient of normal traction stress along an interface or the spherical stress through the bulk lattice is considered as a driving force for diffusion. They argued that if local vacancy equilibrium is maintained throughout the line, the atomic flux divergence is related to the volumetric expansion by:

$$\frac{\partial \ln V}{\partial t} = -\Omega \vec{\nabla} \cdot \vec{J}_a \tag{2.38}$$

where V is local volume element, Ω is atomic volume, $\vec{J}_a$ is atomic flux. In this model, the "thickening" of the interface (line sidewall or grain boundary) is considered and modeled as the insertion of a continuum slab of material having a width u along the boundary

$$\frac{\partial u}{k dt} = -\delta_{path} \Omega \frac{\partial J}{\partial l} \tag{2.39}$$

The stress state along the line is linked to atomic divergence. To avoid computational complexity, the stress field solution near a grain boundary is pre-calculated and then superimposed along all the diffusion paths to find the total stress field. In this work, a void formation and growth model is also proposed.

Bower and Freund (Bower and Freund 1995) developed a computational method to determine the interaction of stress and self-diffusion under electromigration in thin metal lines. The diffusion along the fast diffusion paths of grain boundaries and surfaces is modeled in this work and the deformation is considered using a phenomenological power-law creep constitutive law. By including the curvature-dependent surface energy in the formulation, the migration of voids in the metal line is considered. A finite element methodology is presented that includes diffusion-controlled grain boundary thicknesses as displacement jumps in the weak form of the mechanical equilibrium equation. The examples completed using the method showed impressive results such as drift and shape changes of voids, migration of conducting material, and the determination of stress distributions due to electromigration. Xia, et al. (Xia et al. 1997) extended this methodology to include the effect of elastic strain energy as a driving force for surface diffusion, however grain boundary were omitted. There is a lot of literature on the subject of void nucleation and evolution during electromigration (Nix and Arzt 1992;Suo and Wang 1994;Suo et al. 1994;Yang et al. 1994;Mahadevan and Bradley 1996).

When modeling electromigration-induced stress evolution, consideration of the stress-dependence of atomic diffusivity is necessary, if an atomic diffusion approach is used. In the Korhonen model, both the stress-independent and stress-dependent diffusivity are considered and they argued that the simulation results turned out to be

similar to each other (Korhonen et al. 1993). However, many researchers (Clement and Thompson 1995;Park and Thompson 1997) have shown the importance of including the stress-dependent atomic diffusivity when describing the stress evolution in a thin metal line due to electromigration. Chizhik et al (Chizhik et al. 2000) discussed the role of stress-dependent atomic diffusivity in greater details and lead to a different estimation of the electromigration incubation period. The increase of the atomic diffusivity in the tensile stress region shortens the incubation period. Stress-dependent atomic diffusivity is considered in many works on electromigration (Trattles et al. 1994;Gleixner and Nix 1999;Gleixner and Nix 1996;Knowlton et al. 1997;Clement 1997;Park et al. 1999).

The behavior of electromigration is dependent on the grain structure in the thin metal lines (Joo and Thompson 1994). This is because grain boundary diffusion is the main diffusion mechanism in metal conductors during electromigration and the effective ground boundary diffusivity is greatly dependent on the featured grain size and its spatial distribution. Knowlton, et al. (Knowlton et al. 1997) investigated the complex dependence of dominant failure mechanism on microstructure of metal lines using a grain growth simulator originally developed by Frost et al (Frost et al. 1990). The continuous shrinkage of metal line width leads to a line width below the median grain size. This results in the "bamboo" or "near-bamboo" grain structure in the metal line. A bamboo grain structure means that the metal line is segmented by individual grains and each segment grain covers the whole width of the line. In a bamboo structured metal line, there are no interconnected fast grain boundary diffusion pathes; therefore, the stress evolution is different and it often has a longer electromigration lifetime. Electromigration in bamboo or near-bamboo structured metal lines is one of the current interesting research

topics (Bohm et al. 2002;Sasagawa et al. 2001;Hau-Riege and Thompson 2001;Fayad et al. 2001;Fayad et al. 2000;Zehe and Ramirez 2000;Gleixner and Nix 1998;Liu and Diefendorf 1997;Thouless 1996;Kusuyama et al. 1996;Marieb et al. 1995).

2.3 Research on Electromigration in Solder Joint

Despite the intensive experimental and theoretical research efforts made on electromigration in thin film metal conductors found in integrated circuits, until recently, little attention has been paid to electromigration in solder joints. This is because the current density in solder joints is relatively low and therefore electromigration is not a reliability concern in most applications. Electromigration in Pb95/Sn5 solder film was first reported in 1979 by Di Giacomo(Di Giacomo 1979). He observed electromigration depletion in solder films subject to various current stressing conditions. It is reported that the total depleted volume grows linearly with time and current density. Di Giacomo also found a threshold current density of 0.45×10^4 A/cm^2 for electromigration depletion. The electromigration in bonding solder as a reliability concern was first reported in 1984 by Mizuishi (Mizuishi 1984), when one of the catastrophic failure modes of both AlGaAs/GaAs and InGaAsP/InP double-heterostructure lasers was related to indium whisker growth due to electromigration in indium solder.

The recent developments of utilizing flip-chip technology in next generation power module packaging and ultra-high density microelectronic packaging make electromigration in solder joints a potential reliability problem in the near future. More research efforts are now focused on the reliability of solder joint under current stressing. In 1998 Brandenburg and Yeh reported the first electromigration studies of flip-chip

solder joints (Brandenburg and Yeh 1998). In this work, flip-chip solder joints were subjected to 0.5~1.5×10^4 A/cm^2 of current stressing at junction temperature levels of 150°C and 175°C. Metallurgical analysis of the solder joints identified solder migration as the primary failure mechanism. They found their solder joints life data had a good fit with Black's equation (Black 1967;Black 1969) and found an activation energy of 0.8 eV and a current density exponent of 1.8.

K. N. Tu and colleagues conducted a lot of research on solder electromigration (Huynh et al. 2001;Lee et al. 2001a;Lee and Tu 2001;Lee et al. 2001b;Liu et al. 2000a;Liu et al. 1999a). They first performed electromigration experiments on Pb/Sn solder strips at a current density of 10^5 A/cm^2 near ambient temperature with different alloy composition (Liu et al. 2000a;Liu et al. 1999a). They found that eutectic solder, with the lowest melting point, had the fastest hillock growth rate at the anode. At the cathode, the void formation occurs in the interphase boundaries and is found to grow initially into the Pb grain before consuming the Sn grain. Later, they conducted electromigration experiments on both Pb/Sn and Lead-free flip-chip solder joints at current density of 10^4 A/cm^2 at 120°C (Lee et al. 2001a;Lee and Tu 2001). Hillocks were observed at the anode and voids at the cathode. The dominant diffusing species was found to be Pb. The diffusion marker technique was used to measure the electromigration flux and calculate the effective charge of atomic diffusion in the solder. Significant phase coarsening was observed during electromigration. Their experiments suggested that the effect of electromigration in SnAg3.8Cu0.7 solder is much smaller that that in eutectic Pb/Sn solder joint. They also argued that the UBM itself, aside from the solder joint,

could be part of the reliability problem of the flip-chip solder joint under electromigration, since it may be dissolved into the solder joint after current stressing (Choi et al. 2002b).

Choi et al (Choi et al. 2001;Choi et al. 2002a) studied the electromigration of eutectic Sn/Pb solder using thin strip-type test structures. Significant changes in the microstructure were observed during the electromigration test at a current density of 4.6~8.7×104 A/cm2 at 80~100°C. From resistance measurements, they calculated that the activation energy of the eutectic SnPb solder for electromigration was about 0.77~0.9 eV. The dominant diffusion paths were through interface and surface, and the dominant migrating element at 100°C was Pb.

Although electromigration in solder joint has already attracted a lot of research attention, our understanding of its failure modes and mechanism is still very rudimentary. There is no physical based model that one could use to predict its reliability. Due to the fact that solder alloys are highly inelastic and solder joints have complex geometry, the established models for electromigration in thin metal films cannot be used for solder joints directly. A great deal of research work still needs to be done in order to fully understand the electromigration process in a solder alloy as well as to develop a physics based solder reliability model.

Chapter 3

Modeling and simulation of electromigration

A finite element simulation of stress evolution in thin metal film during electromigration is presented in this chapter. The electromigration process is modeled by coupled diffusion- mechanical partial differential equations (PDEs). The PDEs are implemented with a plane strain formulation and numerically solved with the finite element (FE) method. The evolutions of spherical stress, each component of the deviatoric stress tensor, and Von Mises' stress were simulated for several cases with different line lengths and current densities. Two types of displacement boundary conditions are considered. The simulation results are compared with Korhonen's analytical model (Korhonen et al. 1993) and Black (Black 1967) and Blech's (Blech and Herring 1976) experimental results.

3.1 Introduction

In a confined metal interconnect line that is laminated on a SiO_2 layer and encapsulated by a dielectric passivation layer, electromigration creates stresses that can retard electromigration. Blech (Blech 1976;Blech and Herring 1976;Blech and Tai 1977) was one of the first to explain the origin of this phenomenon. In his experiments, he discovered a critical product of line length and current density, and below this critical number no electromigration failure was observed. Since then, many researchers have studied the evolution of stress due to electromigration. Kirchheim (Kirchheim 1992)

proposed a physically based model in which generation of stress in grain boundaries during electromigration is caused by the annihilation and generation of vacancies. Korhonen (Korhonen et al. 1993) proposed another physically based analytical model for mechanical stress evolution during electromigration in a confined metal line described by a one-dimensional equation, given below:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}[\frac{D_a B \Omega}{kT}(\frac{\partial \sigma}{\partial x} - \frac{Z^* e \rho}{\Omega} j)] \tag{3.1}$$

where σ is the spherical stress, t is time, D_a is the atomic diffusivity, B is applicable modulus, Ω is atomic volume, k is the Boltzman's constant, T is absolute temperature, Z^* is the effective charge number, e is electron charge, ρ is resistivity, and j is current density. The advantage of this model is that the evolution of spherical stress in the confined line can be calculated in a closed form; however, a disadvantage of this model is that the components of the stress tensor are not available. Therefore, it is not possible to use this model to analyze how the boundary conditions would affect the stress evolution in the line. Clement (Clement 1997;Clement and Thompson 1995) proposed a similar model to Korhonen's in terms of vacancy concentration; and in his model still only spherical stress can be calculated. In both models, the relation between the spherical stress and lattice site concentration change is assumed to be:

$$d\varepsilon^T = \frac{dC_l}{C_l} = -\frac{d\sigma}{B}, \tag{3.2}$$

where ε^T is the change in the volumetric strain due to deposition of atoms at grain boundaries, σ is the spherical stress, C_l is lattice site concentration, and B is a parameter called the applicable modulus which depends on the elastic properties of the metal line and the surrounding material, and on the line aspect ratio. This relationship is based on

Eshelby's(Eshelby 1957) theory on elastic fields of inclusion; thus elastic material property is assumed for metal lines.

Instead of using the immediate relationship between lattice density and spherical stress, other researchers, such as Povirk(Povirk 1997), Rzepka(Rzepka et al. 1997) and Garikipati et al.(Garikipati et al. 2001), employed the idea that diffusion fluxes give rise to volumetric strain, which serves to establish stress fields, and drives stress-migration fluxes. Using a similar concept, Sarychev(Sarychev and Zhinikov 1999) proposed a three-dimensional, self-consistent model of stress evolution during electromigration. In this model, local volume change is assumed to be generated by vacancy migration and generation due to electromigration. The local volume change is then treated as an analog of thermal strain. The stress fields are calculated as a result of volumetric strain induced by electromigration at lattice site. In this approach, the assumption of the elastic material property is no longer necessary, and all the components of a stress tensor, not just spherical stress, are available.

Based on Sarychev's electromigration-deformation constitutive model (Sarychev and Zhinikov 1999), a plane strain formulation is derived in this chapter. Finite element simulation is performed for confined Aluminum (Al) lines with different lengths and current densities. Two types of displacement boundary conditions are considered. The spherical stress evolution in the simulation agrees well with Korhonen's(Korhonen et al. 1993) analytical model. The effect of displacement boundary conditions on stress evolution is discussed. Finally, the results are discussed by comparison to Black(Black 1967) and Blech's (Blech and Herring 1976) experimental results.

3.2 Vacancy diffusion and mechanically coupled electromigration model

The electromigration process is an electron flow assisted diffusion process. In this work, the process is assumed to be controlled by a vacancy diffusion mechanism, in which the diffusion takes place by vacancies switching lattice sites with adjacent atoms.

The vacancy diffusion equation of electromigration that considers the concurrent mechanical stress was proposed by Kirchheim as (Kirchheim 1992):

$$\frac{\partial C_v}{\partial t} = -\vec{\nabla} \cdot \vec{q} + G \tag{3.3}$$

and $$\vec{q} = -D_v[\vec{\nabla} C_v + \frac{C_v Z^* e}{kT}(-\rho \vec{j}) - \frac{C_v}{kT}(-f\Omega)\vec{\nabla}\sigma]$$

combined, these two equations become:

$$\frac{\partial C_v}{\partial t} = D_v[\nabla^2 C_v - \frac{Z^* e\rho}{kT}\vec{\nabla}\cdot(C_v \vec{j}) + \frac{f\Omega}{kT}\vec{\nabla}\cdot(C_v \vec{\nabla}\sigma)] + G$$

where C_v, vacancy concentration

D_v, vacancy diffusivity

$\vec{q}$, vacancy flux vector

Z^*, vacancy effective charge number

e, electron charge

ρ, metal resistivity

$\vec{j}$, current density vector

f, vacancy relaxation ratio

Ω, atomic volume

$k = 8.62\times10^{-5} eV/K = 1.38\times10^{-23} J/K$, Boltzman's constant

T, absolute temperature

$\sigma = trace(\sigma_{ij})/3$, hydrostatic or spherical part of the stress tensor

$G = -\dfrac{C_v - C_{ve}}{\tau_s}$, vacancy generation rate (Sarychev and Zhinikov 1999)

$C_{ve} = C_{v0} e^{\frac{(1-f)\Omega\sigma}{kT}}$, thermodynamic equilibrium vacancy concentration

C_{v0}, equilibrium vacancy concentration in the absence of stress

τ_s, characteristic vacancy generation/annihilation time

If we define $C \equiv C_v / C_{v0}$ as the normalized concentration, then the vacancy diffusion equation could be re-written as:

$$\frac{\partial C}{\partial t} = D_v[\nabla^2 C - \frac{Z^* e\rho}{kT}\vec{\nabla}\cdot(C\vec{j}) + \frac{f\Omega}{kT}\vec{\nabla}\cdot(C\vec{\nabla}\sigma)] + \frac{G}{C_{v0}} \qquad (3.4)$$

where, initially, $C = 1 (\text{or } C_v = C_{v0})$.

The vacancy can be considered as a substitutional species at the lattice site with a smaller relaxed volume than the volume of an atom. When a vacancy switches lattice site with an atom or a vacancy is generated/annihilated at a grain boundary or at a dislocation, a local volumetric strain at lattice site occurs. As proposed by Sarychev (Sarychev and Zhinikov 1999), the vacancy diffusion causes volumetric strain at lattice site in the metal during current stressing. This volumetric strain is composed of two parts, ε_{ij}^m, the volumetric strain due to vacancy flux divergence, and ε_{ij}^g, the volumetric strain due to vacancy generation. Since diffusion is a time dependent process, these volumetric strains are naturally expressed in the form of strain rates:

$$\dot{\varepsilon}_{ij}^{m} = \frac{1}{3} f \Omega \vec{\nabla} \cdot \vec{q} \delta_{ij} \tag{3.5}$$

$$\dot{\varepsilon}_{ij}^{g} = \frac{1}{3} (1-f) \Omega G \delta_{ij} \tag{3.6}$$

where δ_{ij} is the Kronecker's symbol.

Thus, the combined volumetric strain rate due to current stressing is:

$$\dot{\varepsilon}_{ij}^{elec} = \dot{\varepsilon}_{ij}^{m} + \dot{\varepsilon}_{ij}^{g} = \frac{\Omega}{3} [f \vec{\nabla} \cdot \vec{q} + (1-f) G] \delta_{ij} \tag{3.7}$$

The total volumetric strain rate due to current stressing is then:

$$\dot{\varepsilon}^{elec} = \Omega [f \vec{\nabla} \cdot \vec{q} + (1-f) G] \tag{3.8}$$

By analogy to thermal strain (which is the volumetric strain caused by temperature variation), the volumetric strain caused by the current stressing is superimposed onto the strains tensor with strains due to other loadings. Thus total strain can be given by:

$$\varepsilon_{ij}^{total} = \varepsilon_{ij}^{mech} + \varepsilon_{ij}^{therm} + \varepsilon_{ij}^{elec} \tag{3.9}$$

where ε_{ij}^{total} is the total strain tensor, ε_{ij}^{mech} is the strain due to mechanical loading, ε_{ij}^{therm} is the strain due to thermal load, and ε_{ij}^{elec} is the volumetric strain due to electromigration.

3.3 Plane strain formulation for the elastic mechanical stress-strain model

A plane strain formulation based on Sarychev's model is derived for simulating the stress evolution in a heavily passivated Al thin film. When an Al line is covered by a heavy passivation layer, the out-of plane displacements are greatly restricted. Therefore, the plane strain assumption that the out-of plane strain is assumed to be zero provides a

good approximation. The standard strain (ε_{ij}) – displacement (u,v,w) relationship is given by:

$$\varepsilon_x = \frac{\partial u}{\partial x}, \varepsilon_y = \frac{\partial v}{\partial y}, \varepsilon_z = \frac{\partial w}{\partial z} \tag{3.10}$$

$$\gamma_{xy} = \frac{\partial u}{\partial y} + \frac{\partial v}{\partial x}, \gamma_{xz} = \frac{\partial u}{\partial z} + \frac{\partial w}{\partial x}, \gamma_{yz} = \frac{\partial v}{\partial z} + \frac{\partial w}{\partial y} \tag{3.11}$$

where, $\varepsilon_z = \gamma_{xz} = \gamma_{yz} = 0$ for the plane strain case constitutive relationship with the mechanical, thermal, and electric current loadings from (3.9) is then:

$$\varepsilon_x = \frac{1}{E}\{\sigma_x - \nu(\sigma_y + \sigma_z)\} + \alpha\Delta T + \frac{\varepsilon^{elec}}{3} \tag{3.12}$$

$$\varepsilon_y = \frac{1}{E}\{\sigma_y - \nu(\sigma_x + \sigma_z)\} + \alpha\Delta T + \frac{\varepsilon^{elec}}{3} \tag{3.13}$$

$$\varepsilon_z = \frac{1}{E}\{\sigma_z - \nu(\sigma_x + \sigma_y)\} + \alpha\Delta T + \frac{\varepsilon^{elec}}{3} \tag{3.14}$$

$$\gamma_{xy} = \frac{1}{G}\tau_{xy}, \gamma_{xz} = 0, \gamma_{yz} = 0 \tag{3.15}$$

where

$$\tau_{xz} = \tau_{yz} = 0 \tag{3.16}$$

$$\varepsilon_z = 0 \tag{3.17}$$

E is Young's modulus

ν is Poisson's ratio

α is the coefficient of thermal expansion

G is shear modulus

Thus:

$$\sigma_z = \nu(\sigma_x + \sigma_y) - E(\alpha\Delta T + \frac{1}{3}\varepsilon^{elec}) \tag{3.18}$$

$$\Rightarrow \quad \varepsilon_x = \frac{1-\nu^2}{E}(\sigma_x - \frac{\nu}{1-\nu}\sigma_y) + (1+\nu)(\alpha\Delta T + \frac{1}{3}\varepsilon^{elec}) \tag{3.19}$$

$$\varepsilon_y = \frac{1-\nu^2}{E}(\sigma_y - \frac{\nu}{1-\nu}\sigma_x) + (1+\nu)(\alpha\Delta T + \frac{1}{3}\varepsilon^{elec}) \tag{3.20}$$

Then

$$\sigma_x = \frac{E}{(1+\nu)(1-2\nu)}[(1-\nu)\varepsilon_x + \nu\varepsilon_y - (1+\nu)(\alpha\Delta T + \frac{1}{3}\varepsilon^{elec})] \tag{3.21}$$

$$\sigma_y = \frac{E}{(1+\nu)(1-2\nu)}[(1-\nu)\varepsilon_y + \nu\varepsilon_x - (1+\nu)(\alpha\Delta T + \frac{1}{3}\varepsilon^{elec})] \tag{3.22}$$

$$\tau_{xy} = G\gamma_{xy} \tag{3.23}$$

And the spherical stress can be calculated as:

$$\sigma = \frac{\sigma_x + \sigma_y + \sigma_z}{3} = \frac{1}{3}\{(1+\nu)(\sigma_x + \sigma_y) - E(\alpha\Delta T + \frac{1}{3}\varepsilon^{elec})\} \tag{3.24}$$

where $\dot{\varepsilon}^{elec}$ is coupled with the vacancy migration and vacancy generation:

$$\dot{\varepsilon}^{elec} = \Omega[f\vec{\nabla}\cdot\vec{q} + (1-f)G] \tag{3.25}$$

Please note that the G in Equation (3.23) represents shear modulus; however, G in Equation (3.25) represents vacancy generation rate. Quasi-static mechanical equilibrium equations for plane strain problem are given by:

$$\frac{\partial\sigma_x}{\partial x} + \frac{\partial\tau_{xy}}{\partial y} = 0 \tag{3.26}$$

$$\frac{\partial\tau_{xy}}{\partial x} + \frac{\partial\sigma_y}{\partial y} = 0 \tag{3.27}$$

Thus, by solving the coupled diffusion-mechanical equations (vacancy diffusion equation (3.3), volumetric strain evolution equation (3.25), and quasi-static mechanical equilibrium equations (3.26) and (3.27)), the stress evolution during electromigration can be obtained. With this model, each component of stress or strain tensor can be calculated. This is opposed to 1-D analytical models such as Korhonen's (Korhonen et al. 1993) where only a global average spherical stress can be calculated. We can also calculate the Von Mises stress field to detect if the material enters the plastic range. The proposed model allows the consideration of different displacement boundary conditions and irregular shaped interconnect lines due to versatility of the finite element methods.

3.4 FEM simulation of the thin aluminum line

FlexPDE is used as the finite element code in the analysis (2002). *FlexPDE* applies integration by parts to reduce second order terms in the partial differential equation (PDE) system to create Galerkin equations. It then differentiates these equations to form the Jacobian coupling matrix. This produces flux integral terms along all sides of each cell. These terms are assumed to be continuous across all interfaces, so that when the Galerkin equations are solved, the solution is consistent with the assumption of flux continuity within the numerical accuracy of the solution, and within the ability of the finite element basis functions to follow the solution shape. *FlexPDE* uses a Newton-Raphson iteration process to solve nonlinear systems. Adaptive mesh refinement is used to reduce the cell size in areas of sharp curvature of the solution. The system iterates the mesh refinement and solution until a user-defined error tolerance is achieved.

In this analysis, the transient stress evolutions of Al thin film with lengths from $25\mu m$ to $100\mu m$ and current densities from 0.5×10^6 to $2\times10^6 A/cm^2$ are simulated. The temperature is assumed to be uniform to eliminate thermally induced stress in the simulations. The complete FlexPDE code for this simulation is listed in Appendix A-1.

3.4.1 Boundary Conditions

A blocking boundary condition for diffusion is assumed, such that the diffusion flux is zero at each end, as well as at both sides of the line. The displacement boundary conditions on the both ends of the Al line are such that both displacements *u* and *v* are fixed. For the two sides of the line, two types of boundary conditions are considered (Figure 11). Type I is such that both displacements *u* and *v*, in the directions of *x* and *y*, respectively, are fixed; Type II is such that only the displacement perpendicular to the side of the line, *v*, is fixed and displacement along the direction of the line, *u*, is allowed. The Type II boundary condition is considered for the case when the passivation layer is not sufficiently strong to restrict slipping between the itself and Al line.

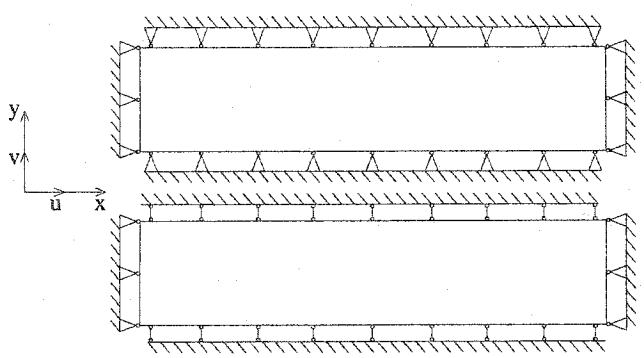


Figure 11 Two types of boundary conditions: top) Type I; bottom) Type II.

3.4.2 Initial Conditions

The initial condition for vacancy diffusion is that the vacancy concentration everywhere equals the equilibrium value for a stress free state. The line is also initially assumed to be strain-free.

Calculation Parameters

Simulation parameters are:

T=473K, temperature (assumed uniformly distributed).

$k = 8.62\times10^{-5} eV/K = 1.38\times10^{-23} J/K$, Boltzman's constant

E=66GPa, Young's modulus of Al

v=0.35, Poission's ratio

$C_{v0} = 6.02\times10^{15}/cm^3$, equilibrium vacancy concentration at a stress free state at 473K. Calculated from atomic concentration of Al by assuming $C_v/C_a \approx 10^{-7}$ at 473K (Korhonen et al. 1993).

$\Omega = 1.66\times10^{-23}/cm^3$, atomic volume.

$\tau_s = 1.8\times10^{-3} s$, vacancy relaxation time(Sarychev and Zhinikov 1999).

f=0.6, average vacancy relaxation ratio(Sarychev and Zhinikov 1999)

Z^*=4, effective charge number (Tu 1992b)

$\rho = 1.139\times10^{-8}T - 2.07\times10^{-7} ohm\cdot cm$, resistivity of Al

3.4.3 Vacancy diffusivity

$D_v = 2.7\times10^{-6} cm^2/s$, the vacancy diffusivity at 473K, is used in this simulation. Grain boundary diffusion is assumed to be the main diffusion mechanism in

electromigration, and lattice diffusion is not considered since grain boundary diffusivity is orders of magnitude higher at this temperature. Frost's(Frost and Ashby 1982) grain boundary diffusivity for Al, $\delta D_{gb} = 5\times10^{-8} e^{-0.87eV/kT} cm^3/s$, is also used. By assuming an average grain size to be 1 μm (Korhonen et al. 1993), the effective atomic diffusivity is thus:

$$D_a = \frac{\delta D_{gb}}{d} = \frac{8.3\times10^{-8} e^{-0.87eV/kT}}{1\times10^{-4}} cm^2/s \ .$$

The vacancy diffusivity is calculated from the relation (Clement and Thompson 1995) $D_a C_a = D_v C_v$ at the stress free state. By again assuming that $C_v / C_a \approx 10^{-7}$ at $473K$, $D_v = 10^7 D_a = 2.7\times10^{-6} cm^2/s$ at the stress free state. Note that the vacancy diffusivity is not dependent on stress, but atomic diffusivity is dependent on stress since vacancy concentration changes with stress.

3.4.4 Simulation results

For each type of displacement boundary condition along the Al line, 5 cases with varying line lengths were simulated as shown in Table 1. In all the cases, the width of the Al line was $15\mu m$. Such a relatively wide line was chosen to avoid the bamboo or near-bamboo grain structure (few or no boundaries along the line direction) that exists in a much narrower line. In the case of bamboo or near-bamboo grain structured lines, i) the assumption of a universal grain boundary diffusivity for the whole line is not valid any more; ii) since the line is separated by the fast diffusion segments (grain boundaries) and the slow diffusion segments (lattice within the bamboo grain), the diffusion is dependent on the particular grain structure of the line. Although many researchers have explored

electromigration in bamboo structured lines(Han et al. 1999;Gungor and Maroudas 1999;Knowlton and Thompson 1998;Duan and Shen 2000), this is not the focus of the current work. The second reason for choosing a line width of 15μm in the simulation is that it is close to the line width used in Blech's experiments(Blech and Herring 1976;Blech 1976;Blech and Kinsbron 1975). Later we will compare this simulation to his experimental results. The mesh used for FE analysis is shown in Figure 12. The current flow was from left to right.

Table 1 Simulation cases with different line length and current density

	Case I	Case II	Case III	Case IV	Case V
Line length (μm)	25	50	100	50	50
Current density ($10^6 A / cm^2$)	1	1	1	0.5	2

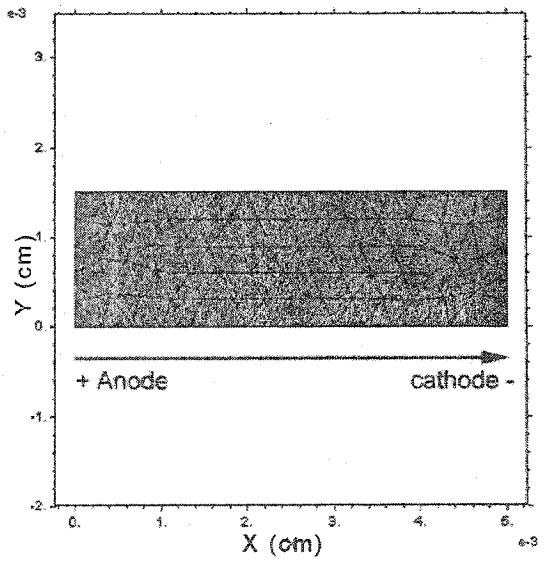


Figure 12 FEA mesh

Results for all cases shown in Table 1 are presented later in a table format. In this part, simulation results for Type I and Case II are presented in Figures 13-27 are discussed in detail. The figures show length in *cm*, stress in N/cm^2, and time in *seconds*.

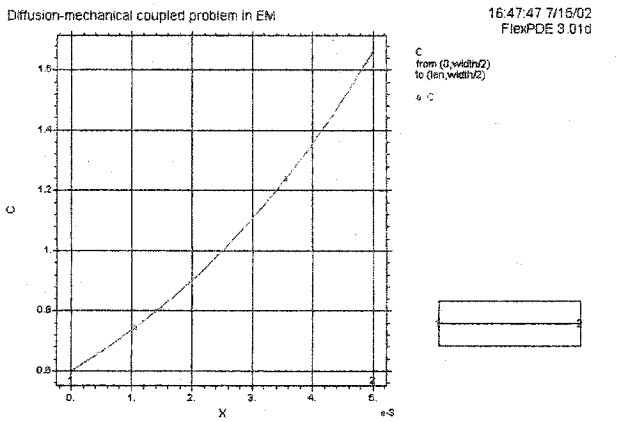


Figure 13 Steady state normalized vacancy distribution along the thin film

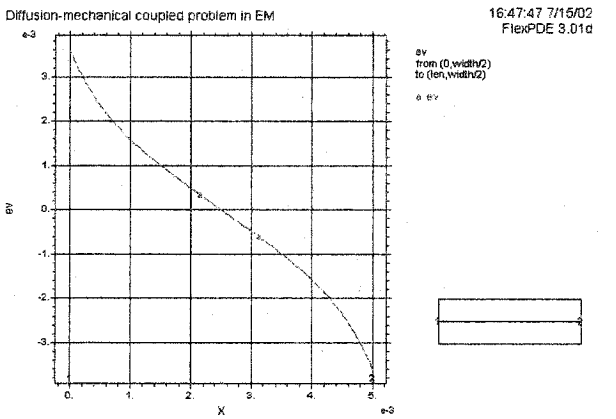


Figure 14 Steady state distribution of volumetric strain along the thin film

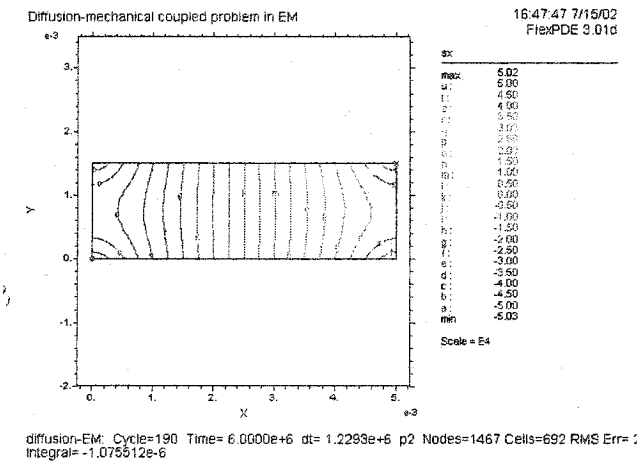


Figure 15 Steady state distribution of axial stress σ_x along the thin film

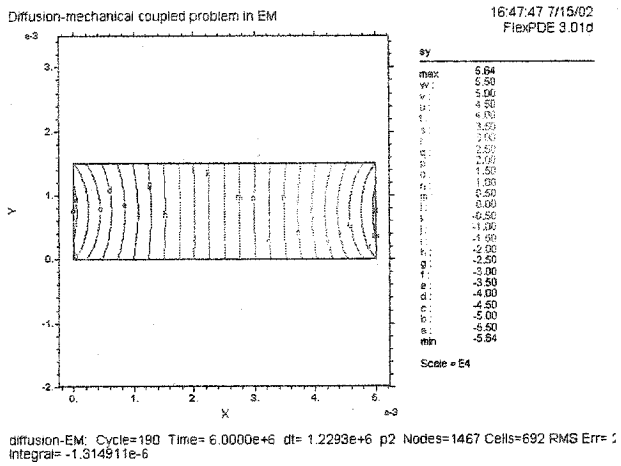


Figure 16 Steady state distribution of transverse stress σ_y along the thin film

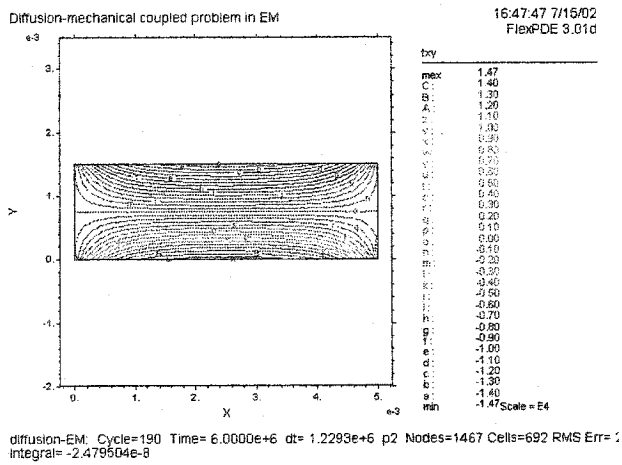


Figure 17 Steady state distribution of shear stress τ_{xy} along the thin film

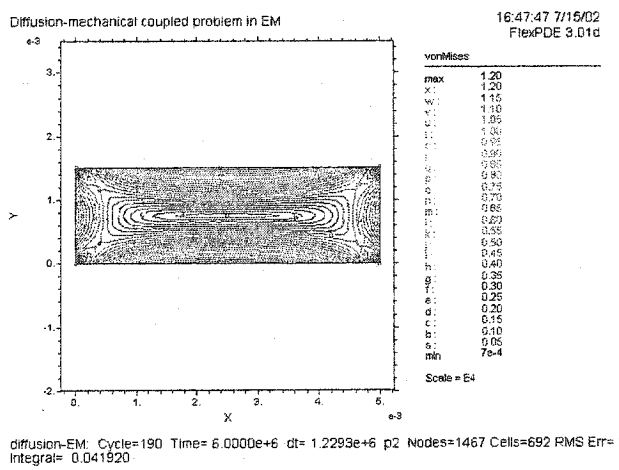


Figure 18 Steady state distribution of Von Mises stress along the thin film

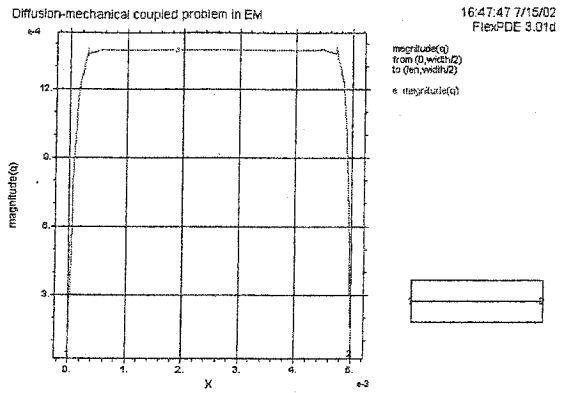


Figure 19 Normalized vacancy flux distribution along the film length after 70 seconds of stressing

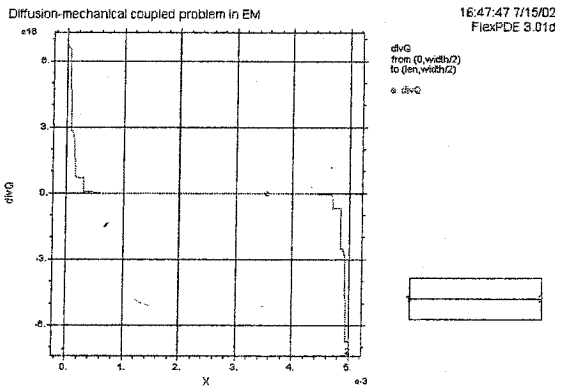


Figure 20 Vacancy flux divergence distribution along the film length after 70 seconds of stressing

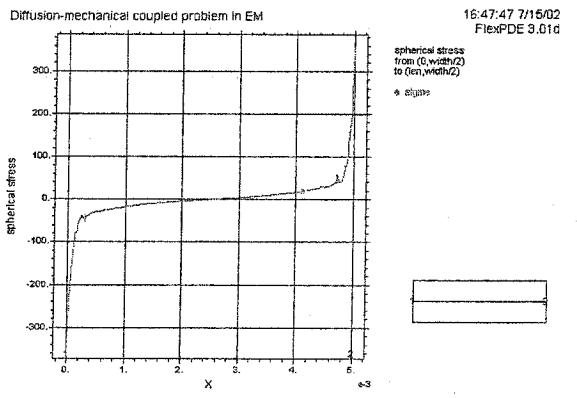


Figure 21 Spherical stress distribution along the film length after 70 seconds of stressing (3.5MPa maximum)

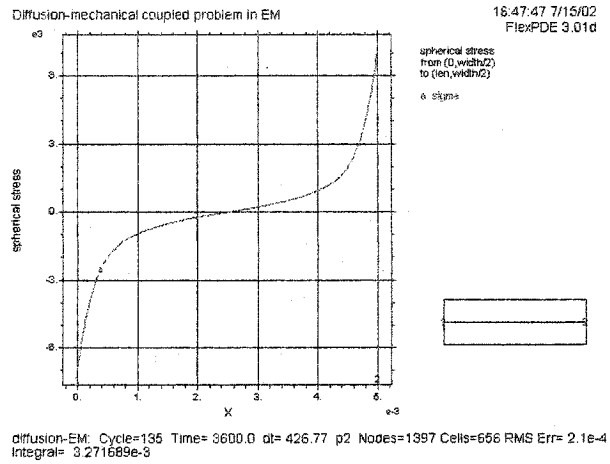


Figure 22 Spherical stress distribution along the film length after 3600 seconds of stressing (70MPa maximum)

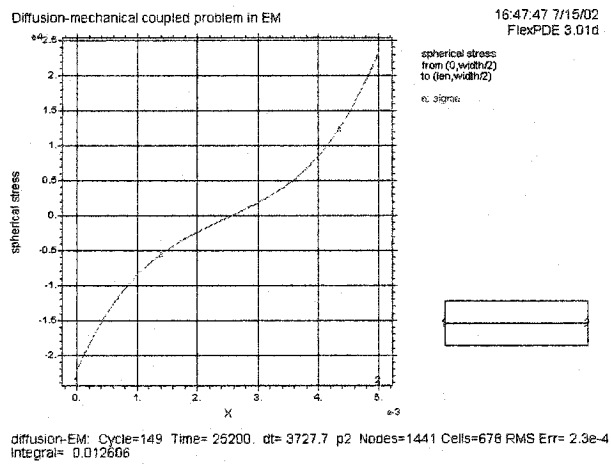


Figure 23 Spherical stress distribution along the film length after 25200 seconds of stressing (230MPa maximum)

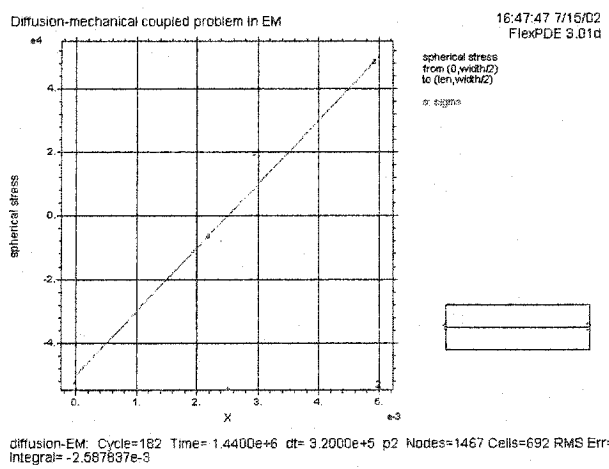


Figure 24 Steady state distribution of spherical stress (500MPa maximum)

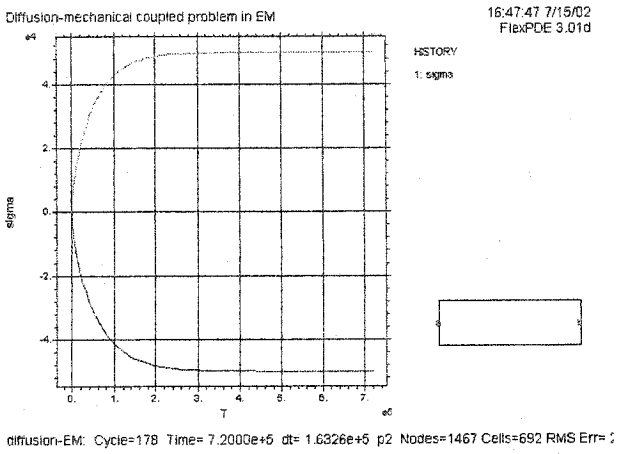


Figure 25 Spherical stress evolution at both ends of the line

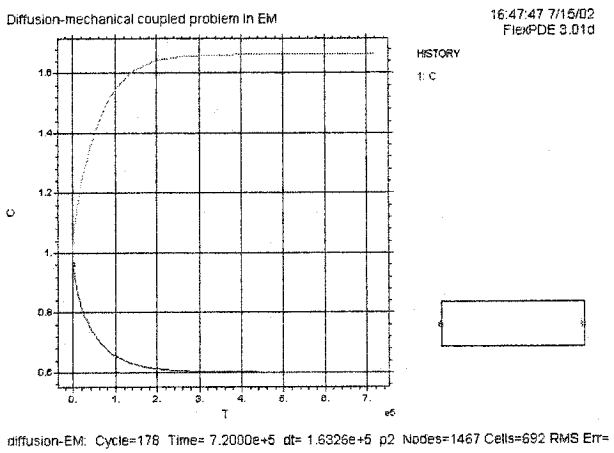


Figure 26 Evolution of normalized vacancy concentration at both ends of the line

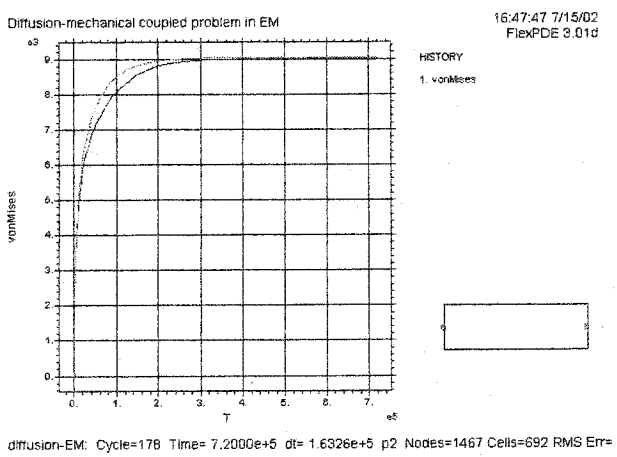


Figure 27 Evolution of Von Mises stress at both ends of the line

At steady state, the vacancy concentration distribution along the line was nearly linear, with the lowest concentration at the anode side (left side) as shown in Figure 13. The steady state volumetric strain (Figure 14) was positive (compressive) near the anode side as ions migrated into and accumulated in this region or vacancies migrated out. It was negative (tensile) near the cathode side. The steady state stress components σ_x, σ_y, and τ_{xy} are shown in Figures 15-17. Since the yielding of metals is independent of the hydrostatic portion of the stress tensor, the value of spherical stress in the Al line is not an adequate measure of whether or not the Al has reached the plastic range. Von Mises stress is often used as the yield condition for metals and is shown in Figure 18. The maximum Von Mises stress value ($120MPa$) is seen along the four edges of the Al line.

Figure 19 shows the normalized vacancy flux distribution along the center of the Al line after 70 seconds of current stressing. The vacancy flux was zero at both ends due to the blocking diffusion boundaries. The corresponding divergence of the vacancy flux is shown in Figure 20. As the diffusion process approaches steady state, the respective vacancy flux divergence gradually decreases to zero.

The evolution of the spherical stress distribution is shown in Figures 21-24. Spherical stress first developed near both ends of the Al line, and then gradually decreased inward. It eventually changed signs in the middle. At steady state, the spherical stress was in compression near the anode side and was in tension near the cathode side.

Time histories at both ends of the Al line for spherical stress, normalized vacancy, and Von Mises stress are shown in Figures 25-27. These values increased with time during current stressing and finally reached steady state at approximately the same time. Both the spherical stress time-history and its distribution evolution are similar to the

results from Korhonen's analytical model (Korhonen et al. 1993). Since this model also gives individual components of the stress tensor, it makes it possible to use appropriate yield conditions to decide where the material enters plasticity. Whereas, Korhonen's (Korhonen et al. 1993) model provides only a global spherical stress value.

3.5 Further Discussion

The simulation results show that electric current stressing creates volumetric strains at lattice site along the Al line due to vacancy flux divergence and vacancy generation/annihilation, as shown in Figure 14. Due to the applied boundary constraints, mechanical stresses develop. A summary of simulation results for the five cases and two types of boundary conditions are shown in the following tables.

Table 2 Summary of simulation results for Type I displacement boundary condition

Case	Current density J ($10^{8} A/cm^{2}$)	strip length L (μm)	Product LxJ (A/cm)	Time to reach steady state (hrs)	Time to reach spherical stress level ($100MPa$)	Time to reach spherical stress level ($300MPa$)	Time to reach vonMises stress level ($40MPa$)	Steady state spherical stress level (MPa)	Steady state vonMises stress level (MPa)
I	1	25	2500	33.3	1.92	****	1.44	250	88
II	1	50	5000	111.1	1.72	11.4	1.61	500	90
III	1	100	10000	444.4	1.69	10.4	1.61	1000	90
IV	0.5	50	2500	111.1	5.56	****	19.4	250	45
V	2	50	10000	111.1	0.57	3.2	0.39	1000	180

Note: **** this stress level was not achieved (same meaning in following tables)
Time is in hours in all the tables

Table 3 Summary of simulation results for Type II displacement boundary condition

Case	Current density J ($10^{8} A/cm^{2}$)	strip length L (μm)	Product LxJ (A/cm)	Time to reach steady state (hrs)	Time to reach spherical stress level ($100MPa$)	Time to reach spherical stress level ($300MPa$)	Time to reach vonMises stress level ($70MPa$)	Steady state spherical stress level (MPa)	Steady state vonMises stress level (MPa)
I	1	25	2500	55.6	3.6	****	3.5	250	175
II	1	50	5000	225.0	3.6	30.6	3.5	500	350
III	1	100	10000	972.2	3.6	30.6	3.5	1000	700
IV	0.5	50	2500	222.2	13.9	****	13.9	250	175
V	2	50	10000	227.8	0.9	7.5	0.9	1000	700

Korhonen (Korhonen et al. 1993) predicted that the time for electromigration to reach a steady state (a state where the atomic or vacancy flux are zero everywhere and thus there is no further stress development) is proportional to the square of the line length. In this simulation, the results show that the time to reach steady state is approximately dependent on the square of the line length as shown in Table 4, which agrees with Korhonen's prediction. The time to reach steady state is independent of current density but dependent on the displacement boundary conditions.

Table 4 Time for electromigration to reach steady state

		Case I	Case II	Case III	Case IV	Case V
Line length (μm)		25	50	100	50	50
Current density ($10^6 A/cm^2$)		1	1	1	0.5	2
Time to reach steady state (hrs)	Type I B.C.	33.3	111.1	444.4	111.1	111.1
	Type II B.C.	55.6	225	972.2	222.2	227.8

If we consider the time to reach certain hydrostatic or Von Mises stress levels at the blocking boundary, the results in Table 5 show that time is mostly dependent on the current density and nearly independent of the Al line length for all simulation cases. For Type I displacement boundary conditions, the time to reach certain spherical stress levels is weakly dependent on the inverse of the square of current density. For example, the time to reach a spherical stress level of $100MPa$ averaged about 1.78 hours for Cases I, II, and III with Type I conditions, where the current density is $10^6 A/cm^2$. When current density is reduced to $0.5\times10^6 A/cm^2$, as in Case IV, the time increases to 5.56 hours, which is 3.1 times as long as Cases I to III. When current density increases to $2\times10^6 A/cm^2$, as in Case V, the time reduces to 0.57 hours, which is 0.32 times as long as Cases I to III. But the time to reach certain Von Mises stress levels is strongly dependent on the inverse of the square of current density, such that $t_\sigma \propto j^{-2}$. For Type II displacement boundary conditions, the times to reach certain spherical stress and Von

Mises stress levels are both strongly dependent on the inverse of the square of current density.

Table 5 Time to reach certain hydrostatic or Von Mises stress level at blocking boundary

		Case I	Case II	Case III	Case IV	Case V
Line length (μm)		25	50	100	50	50
Current density ($10^6 A/cm^2$)		1	1	1	0.5	2
Type I B.C.	Time to reach hydrostatic stress level of 100*MPa* (*hrs*)	1.92	1.72	1.69	5.56	0.57
	Time to reach hydrostatic stress level of 300*MPa* (*hrs*)	****	11.4	10.4	****	3.2
	Time to reach Von Mises stress level of 40*MPa* (*hrs*)	1.44	1.61	1.61	This level is too close to steady state	0.39
Type II B.C.	Time to reach hydrostatic stress level of 100*MPa* (*hrs*)	3.6	3.6	3.6	13.9	0.9
	Time to reach hydrostatic stress level of 300*MPa* (*hrs*)	****	30.6	30.6	****	7.5
	Time to reach Von Mises stress level of 70*MPa* (*hrs*)	3.5	3.5	3.5	13.9	0.9

If we use Korhonen's assumption that the line failure occurs when the spherical stress reaches a critical value, the time to failure of the Al line is at least weakly proportional to the inverse of the square of current density. However, this assumption is not correct since material would not yield under pure spherical stress. It is more appropriate to assume that failure occurs when the Von Mises stress reaches a critical value (e.g. yield condition), since spherical stress cannot be used as a yield condition for metals. In a finite line, if a steady state of electromigration is achieved before yielding, the total steady state flux becomes zero; at this point, the electromigration flux is entirely balanced by the counterflux due to the spherical stress gradient and consequently there will be no further electromigration damage. If Von Mises stress reaches a critical value (yield condition) at the end of the Al line before the steady state flux becomes zero, the blocking boundary region experiences plasticity. This prevents the build up of stress gradient in the Al line which counter-balances the electromigration flux. Thus, zero-flux steady state may never be reached, and the Al line fails. The time for Von Mises stress to reach a critical level is shown to be inversely dependent on the square of current density.

This observation is in accordance with Black's experiments (Black 1967) on metal line electromigration, which showed that MTTF depends on the current density to the power of -2,

$$t_{50} = Aj^{-2}e^{\Delta H/kT} \tag{3.28}$$

where j is the current density, t_{50} is the median time to failure, A is a constant, and ΔH is the activation energy of the failure process.

A more rigorous mechanical constitutive model, such as the viscoplastic model, can be used to track stress evolution and provide a more accurate simulation of this diffusion-mechanical coupled electromigration process. That will be the subject of future work.

Table 6 Steady state hydrostatic and Von Mises stress

		Case I	Case II	Case III	Case IV	Case V
Line length (μm)		25	50	100	50	50
Current density ($10^6 A/cm^2$)		1	1	1	0.5	2
Product LxJ (A/cm)		2500	5000	10000	2500	10000
Steady state spherical stress level (MPa)	Type I B.C.	250	500	1000	250	1000
	Type II B.C.	250	500	1000	250	1000
Steady state Von Mises stress level (MPa)	Type I B.C.	88	90	90	45	180
	Type II B.C.	175	350	700	175	700

The steady state hydrostatic and Von Mises stresses are listed in Table 6 for both Type I and Type II displacement boundary conditions. The steady state spherical stresses are proportional to the product of line length and current density. These results agree with Korhonen's analytical results (Korhonen et al. 1993). The steady state Von Mises stresses are also proportional to the product of line length and current density for Type II displacement boundary conditions; however, for Type I boundary conditions, the steady state Von Mises stresses are only proportional to the current density.

The following conclusion can be reached based on the above assumption that no electromigration failure occurs if electromigration reaches steady state before yielding. Combining Von Mises yield conditions and Type I boundary conditions predicts that electromigration failure occurs above a critical current density, since the steady state Von Mises stress is proportional to current density. Combining Von Mises yield conditions and Type II boundary conditions leads to the prediction that electromigration failure occurs above a critical "product" of current density and line length, since steady state Von Mises stress is proportional to this product. This observation with Type II boundary conditions is in accordance with Blech's experiments (Blech 1976;Blech and Tai 1977), where he found a critical product of line length and current density below which no electromigration failure is observed. Some researchers (Korhonen et al. 1993;Clement and Thompson 1995) use a critical spherical stress value as a failure criterion, which leads to a critical product of current density and line length. I believes this is not appropriate, since a spherical stress level cannot be used as a yield condition for metals, which is the basic tenet of strength of materials theory.

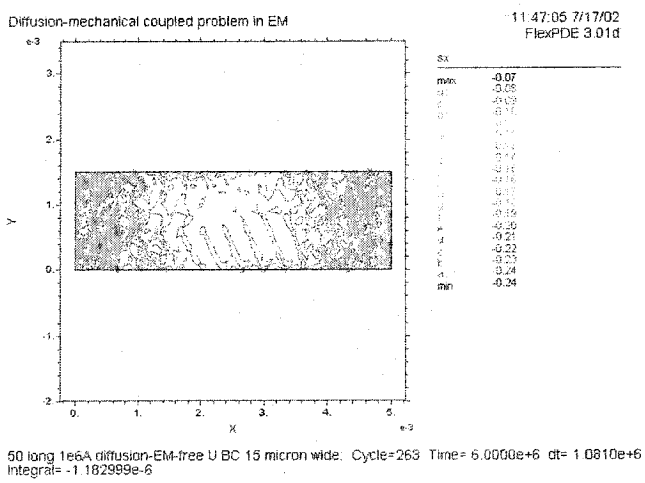


Figure 28 Steady state distribution of axial stress σ_x in Case II with Type II boundary condition

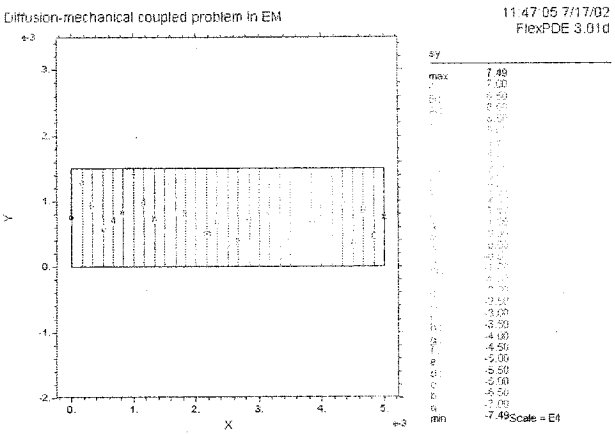


Figure 29 Steady state distribution of transverse stress σ_y in Case II with Type II boundary condition

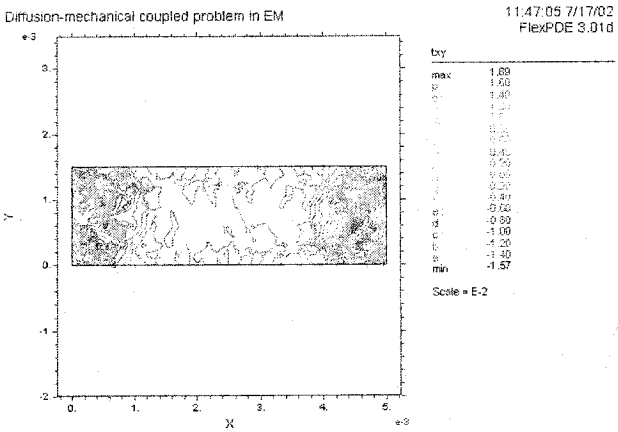


Figure 30 Steady state distribution of shear strains τ_{xy} in Case II with Type II boundary condition

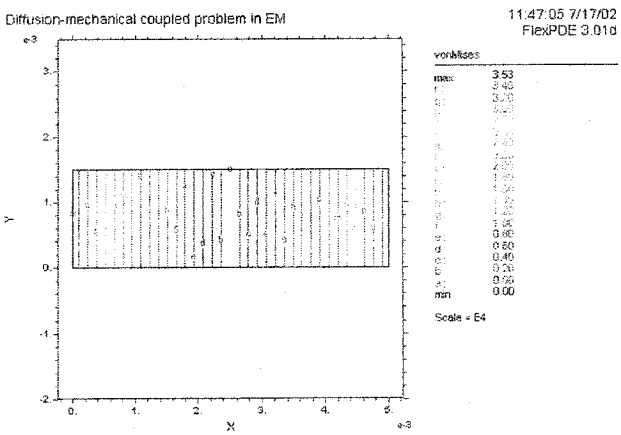


Figure 31 Steady state distribution of Von Mises stress in Case II with Type II boundary condition

The steady state distributions of normal, shear, and Von Mises stress distributions in Case II with Type II boundary conditions are shown in Figures 28-31, as compared to the results from Type I boundary conditions in Figures 15-18. The stress distributions in these two types of boundary conditions are dramatically different. Type I boundaries create a more rigid constraint than Type II. A normal stress gradient of σ_x and a shear stress gradient of τ_{xy} developed for Type I boundary conditions, whereas σ_x and τ_{xy} were almost zero everywhere for Type II boundary conditions. Uniformly constrained Type I boundary conditions in the line also prevent Von Mises stress from getting large. The shear stress along the side of the Al line for Type I boundary conditions was very high, and may well exceed the shear strength between the Al line and its passivation surroundings.

3.6 Conclusions

In this chapter partial differential equations (PDEs) for diffusion-mechanical coupled electromigration processes are solved using the finite element method. The PDE system is based on vacancy diffusion-mechanical coupled process. The results indicate that boundary conditions and current density greatly influence the process of electromigration. The results have been compared qualitatively against experimental results published in the literature and an analytical model by Korhonen. Simulation results indicate that by controlling the boundary conditions, electromigration induced damage can be mitigated.

The simulation results also demonstrate that this PDE system is capable of modeling an electromigration process without the particular assumptions of mechanical material properties and conductor geometry or boundary conditions. In the Chapter 4, this PDE system will be extended to modeling electromigration in a solder joint.

Chapter 4 Moiré Interferometry Experiment on BGA Solder Joint under Current Stressing and Numerical Simulation

Understanding the strain evolution in the solder joints over time while it is under current stressing is an important step toward developing a model. In this chapter, the Moiré Interferometry technique (Post et al. 1994) is used to measure real-time, full-field displacement in the solder joint during electrical current stressing under in-situ conditions.

In the first section, a preliminary experiment on a eutectic Pb/Sn solder joint is presented. A finite element model (FEM) simulation for thermal stresses was performed and compared with the measured strain. The initial results show that the measured strain was largely due to thermal stressing for the current density of 1.8×10^2 A/cm^2. In the following section, the improved Moiré Interferometry experiments with temperature control distinguishes deformation of solder joint due to pure current stressing above 5000 A/cm^2. The electromigration constitutive model presented in Chapter 3 is applied to modeling the deformation of solder joint under current stressing. The numerical simulation results agree well with the experimental results.

4.1 Preliminary Experiment

The development of a constitutive model is sought to predict the stress-strain field in a solder joint undergoing high-density electrical current flow. As a first step, the strain field in a BGA solder ball was measured using Moiré Interferometry. Strain evolution was derived with a natural cubic-spline interpolation method. Previous work reported

electromigration damage in solder joints undergoing current stressing of about 1.3 X 10^4 A/cm^2 at ambient room temperature (Lee et al. 2001a;Brandenburg and Yeh 1998;Ye et al. 2002a). However, preliminary testing results presented here indicate that reliability may be greatly diminished at current densities much less than that due to complications from thermal stressing.

The size of the tested solder joint was 3.8 mm in diameter and 1.70 mm in height. The maximum current applied to the solder joint was 10 Amp yielding a computed density of 175 A/cm^2. This density is much lower than the one needed to trigger electromigration; as reported in the literature (Lee et al. 2001a;Brandenburg and Yeh 1998;Ye et al. 2002a). A FEM simulation of thermal stressing was performed and validated by experimental results, indicating that the strain under such current density was mostly due to thermal stresses.

4.1.1 Experimental Set-up

This research focuses solely on the reliability of solder joints. Hence, two thick copper plates form the test vehicle module instead of an FR4 carrier substrate and silicon die. The advantage of the thick copper plates as substrates is that the electrical connection can be made very simply and can carry a fairly large electrical current. A schematic diagram of the test vehicle is shown in Figure 32(a, b). A thin silicon dioxide layer was used as the solder mask on the copper plate.

The dimension of the copper plate is 40*mm* by 40*mm*. The copper plate was firstly polished with 1200 grit abrasive paper to eliminate the oxidation. A continuous silicon dioxide layer (1μm in thickness) was deposited on the copper plate using a depositing machine. A layer of photoresist was then spin-coated on top of the silicon dioxide layer.

A photolithography process was followed to pattern the photoresist layer. Finally, hydro-fluoride acid was used to remove the silicon dioxide in order to expose copper surface at the positions where solder joints would be reflowed. The photolithography process was done in a class 1000 clean room. A hot plate was used to reflow the eutectic Pb37/Sn63 alloy solder to form interconnect spheres. Spacers were used during reflow. Some oxidation of the copper was observed. The size of the tested solder joint was 3.8mm in diameter and 1.7mm in height.

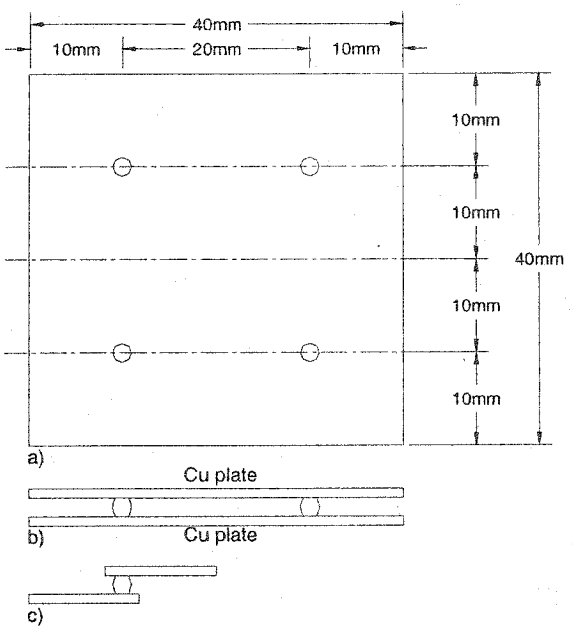


Figure 32 The schematic diagram of the Test Vehicle (a) plane view and (b) side view (c) test vehicle after cross-sectioned with a diamond wheel saw

The test vehicle was first sliced through the center of the solder joint with a high precision diamond-wheel saw. It was further sliced to the shape that could be fit into the fixture (Figure 32), and polished with 200-, 600-, and 1200-grit abrasive paper. An optical diffraction grating was replicated on the sectioned surface.

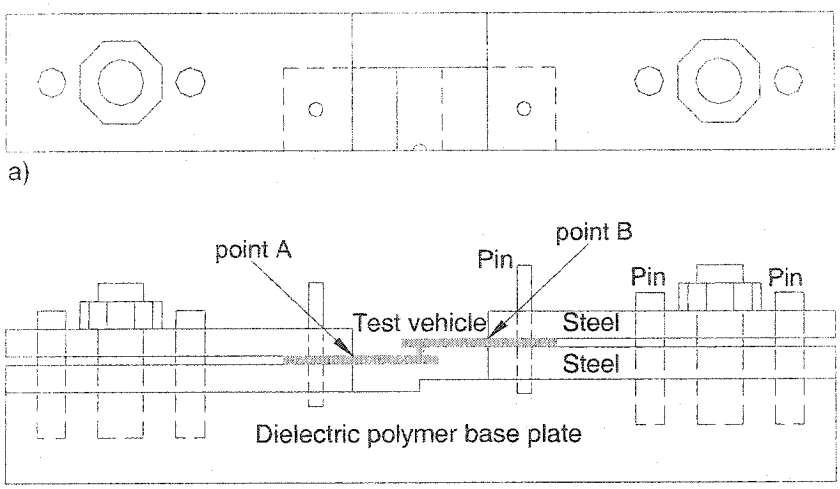


Figure 33 The schematic diagram of the test vehicle fixture (a) plane view (b) the front view

The fixture is composed of a dielectric polymer base plate with two steel plates on each end. The steel plates are affixed by screws and positioned via pins. The test vehicle was then clamped between the two steel plates and positioned by the pins. Electrical-test connections were made through the steel plates. The schematic diagram of the test vehicle fixture is shown is Figure 33.

A schematic diagram of the experimental test set-up is shown in Figure 34. In this set-up, the current was applied by the H-P6260B power supply. The output of this power supply can either be set from its front panel if only constant current is needed, or can be remote controlled by a computer through an H-P59501B DAC if a current profile is needed. The current applied through the test vehicle was monitored using a microvolt meter by a Kelvin connection to a serial resistor. An OMEGA infrared temperature sensor monitored the temperature on the top surface of the test module. The DAC and microvolt meters were connected to the computer through IEEE 488 interface. All the controls, measurements and data logging were implemented in a Labview® user

subroutine (Figure 35). The monitored temperature is later used in the FEM thermal stress analysis.

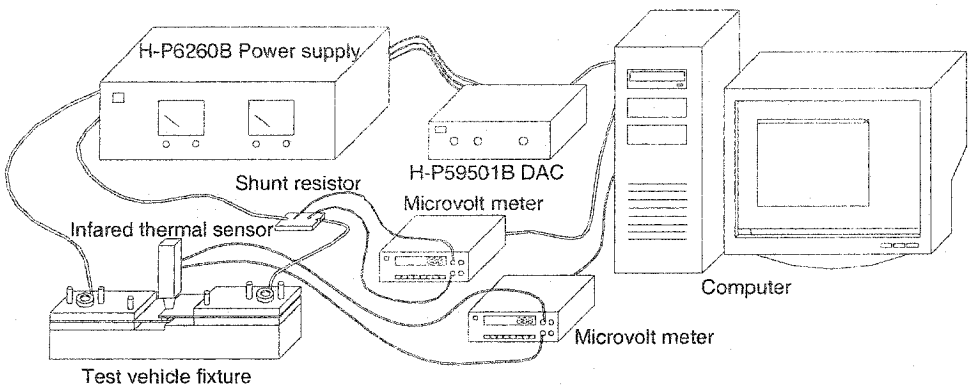


Figure 34 Schematic diagram of the test set-up

The module is mounted onto the Moiré Interferometry table and all wiring connected as shown. The optical set-up is then tuned to get a null field. Since Moiré Interferometry measurement relies on an initial reference field, the optical set-up was carefully protected from any disturbance during testing.

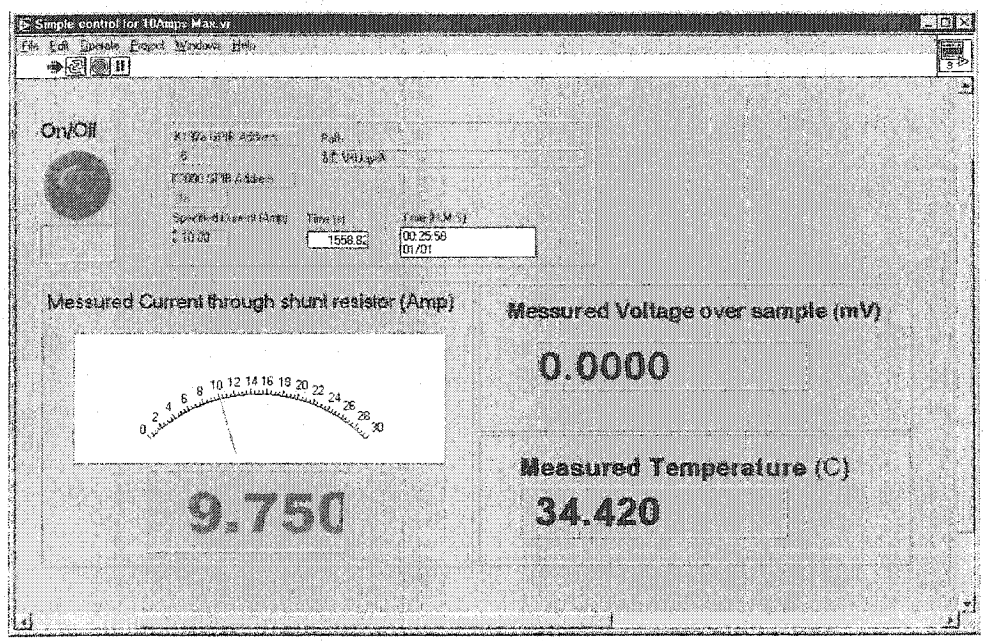


Figure 35 Labview control interface

The Moiré Interferometry technique is explained extensively by Post (Post et al. 1994). The development of the imaging systems used for submicron displacement measurement using Moiré Interferometry technique has been described in detail in Zhao et al. (Zhao et al. 1999; Zhao et al. 2000). The major advantage of Moiré Interferometry is its high sensitivity, high resolution, and whole field view of the deformation distribution of the specimen surface. The optical diffraction grating (with a frequency of 1200 lines/mm) is replicated on the specimen surface. The specimen grating diffracts the incident two coherent laser beams with certain incident angle, and in the direction normal to the specimen surface, two strong diffracted beams are obtained. When the specimen surface deforms, the optical diffraction grating deforms with it, and the two diffracted beams in the normal direction generate an interferometry pattern that represents the in-plane displacement distribution. This scheme applies to both the horizontal and vertical direction, so that deformation in the two perpendicular directions can be obtained. The feature fringe pattern generated by the two vertical beams represents the vertical deformation field, and the fringe pattern generated by the two horizontal beams represents the horizontal deformation field (Zhao et al. 2000).

4.1.2 Experimental Results

The test module was first energized with 5.8 *A* of DC current for 20 minutes. The current was then raised to 9.8 *A*, as shown in Figure 36. The total current stressing time was 4 *hours*. The Moiré interferometry fringes of both U and V fields were recorded in real time. After the current was turned off, deformation fringes were recorded for another 17 *hours*.

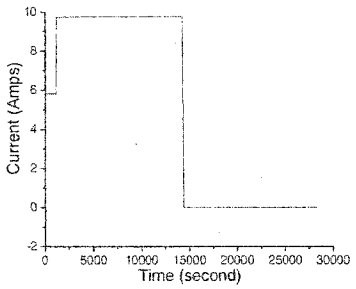


Figure 36 Profile of the current applied

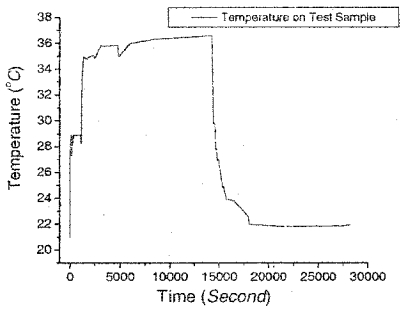


Figure 37 Measured temperature time history

Figure 37 shows the solder joint temperature time history measured by the infrared temperature sensor. The solder joint temperature increased from room temperature to $29^{\circ}C$ immediately due to joule heating and remained there until the current was increased to 9.8 A. The temperature abruptly increased to $34^{\circ}C$ and gradually rose to $36.5^{\circ}C$. After the current was turned off, the temperature abruptly decreased to $29^{\circ}C$ and progressively decreased to room temperature in an hour.

The temperature that is measured with the infrared thermal sensor (with a spotsize of $10mm$ in diameter) is the average temperature of the central area on the top surface of the test module. A fine thermo-couple was also used to pinpoint the temperature distribution on the module during current stressing. The temperature distribution was not uniform. An appreciable heat source was found at the interface of the copper plates and clamping fixture, and needed to be included in the analysis. When the temperature atop

the copper plate was 36.5°C, the temperature near the ends of copper plates increased to 57°C (points A and B in Figure 33).

Figure 38 and Figure 39 are the initial Moiré interferometry fringes of the solder joint before current stressing for the U and V fields, respectively. The initial fringes and non-uniformity indicates initial strains during the sample mounting process. Figures 40-43 show the Moiré interferometry fringe evolution with time during and after current stressing.

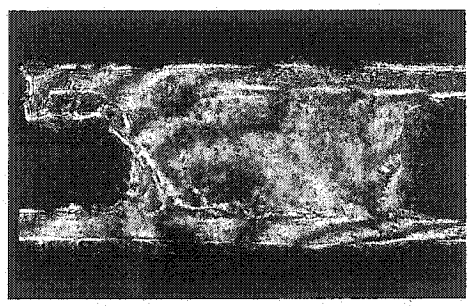


Figure 38 Initial U field

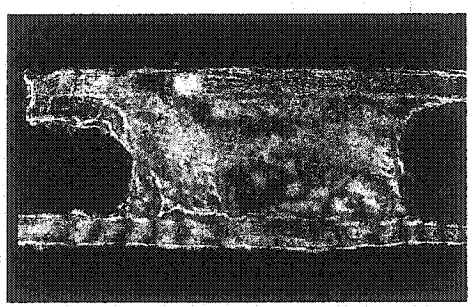


Figure 39 Initial V field

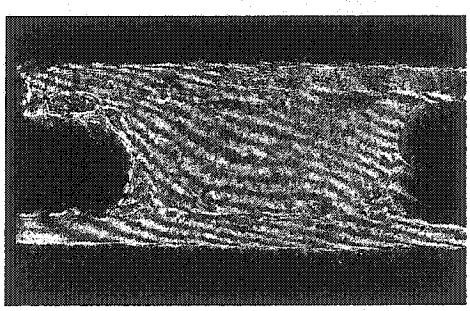


Figure 40 U field (after 02h:22m:0s of stressing)

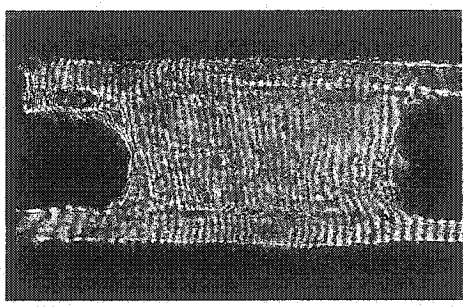


Figure 41 V field (after 02h:22m:15s of stressing)

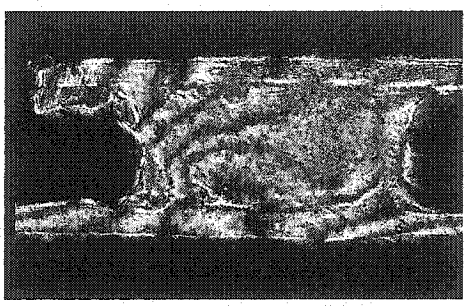


Figure 42 U field (2h:0m:0s after current turned off)

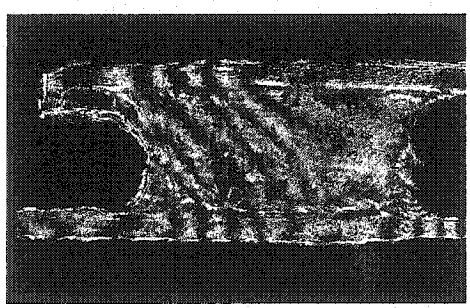


Figure 43 V field (2h:0m:15s after current turned off)

4.1.3 Strain Analysis

To extract the strains from the Moiré interferometry fringes, determination of the direction of the fringe order is needed. During the experiment, the test module was perturbed in the $+x$ direction (coordinates as shown in Figure 44) and the fringes moved toward the direction of lower-order fringes (Post et al. 1994). The direction of fringe order, N_y was determined similarly by $+y$ direction perturbation and observing the direction of the V field movement.

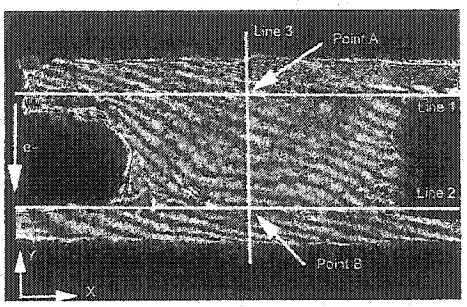


Figure 44 Lines of interest and position of point A, B

Once the fringe orders N_x and N_y are determined, the strains at any point are given by,

$$\varepsilon_x = \frac{\partial U}{\partial x} = \frac{1}{f}[\frac{\partial N_x}{\partial x}]$$
$$\varepsilon_y = \frac{\partial V}{\partial y} = \frac{1}{f}[\frac{\partial N_y}{\partial y}]$$
$$\gamma_{xy} = \frac{\partial U}{\partial y} + \frac{\partial V}{\partial x} = \frac{1}{f}[\frac{\partial N_x}{\partial y} + \frac{\partial N_y}{\partial x}] \qquad (4.1)$$

Where N_x and N_y are fringe orders in U and V fields, respectively, and $f = 2f_x$, f_x is the frequency of diffraction grating (1200 *lines/mm*). With this frequency, the resolution of displacement is $0.417\mu m$ for every fringe order. Instead of using linear interpolation, natural cubic spline interpolation is used to more accurately approximate the derivative of fringe order.

Three lines of interest are shown in Figure 44. The distribution of ε_x is extracted along horizontal Line1 and Line 2. Similarly, the distribution of ε_y is extracted along Line 3. However, the shear strain γ_{xy} is only extracted for points A and B. These points are chosen because they are located near the interface of the solder and copper plate on the solder side. This process is repeated for U and V fringe patterns at specific times, thus producing the strain evolution with time.

Strain fields are extracted from the Moiré interferometry fringes that were recorded after 1hr:40min of current stressing. The resolution of fringes in the copper precludes measurement of that U field, therefore, only the ε_x field of the solder joint is

extracted as shown in Figure 45. The distribution of ε_y and γ_{xy} are plotted in Figures 46 and 47 including both the copper plate and solder joint. The upper and lower copper plates are 0.4 *mm* thick. The ε_x is in expansion everywhere on the solder joint, while ε_y is mostly in contraction within the joint and in expansion within the two copper plates. The largest shear strain is observed near the center of the solder joint.

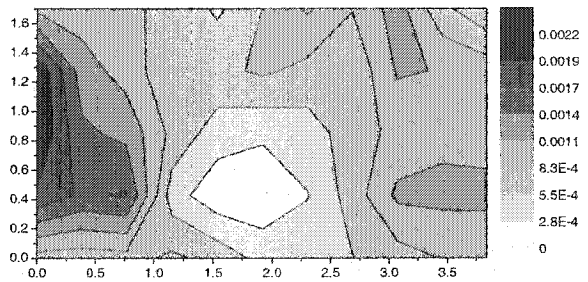


Figure 45 Normal Strain ε_x distribution after 1h:40m of current stressing

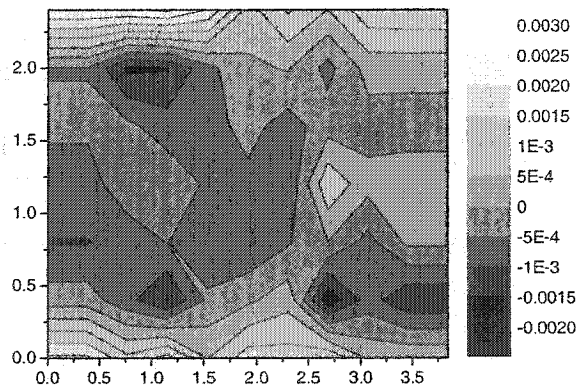


Figure 46 Normal Strain ε_y distribution after 1h:40m of current stressing

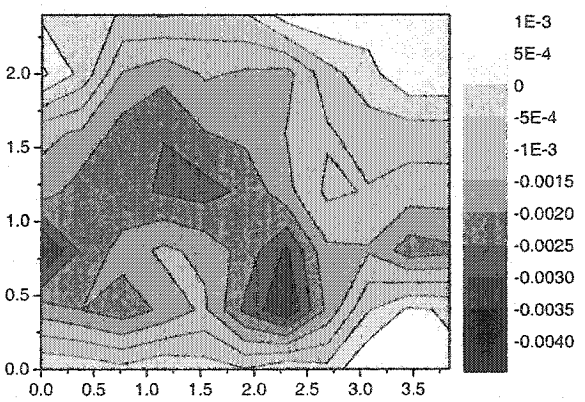


Figure 47 Shear Strain γ_{xy} distribution after 1h:40m of current stressing

4.1.4 FEM Thermal Stress Analysis

To assess the contribution of thermal stresses to the strains in the solder joint, a FEM simulation is performed with ANSYS finite element code and compared to Moiré Interferometry measurements. A uniform temperature change from 22 ^oC to 37^oC is applied to the solder joint and its vicinity. A higher temperature change from 22 ^oC to 57^oC is applied to both ends of the copper plate to account for local heating due to the high contact resistance between the copper plates and the fixture. The model geometry is shown in Figure 48. Since the thickness of the sectioned solder joint is less than 2*mm* compared to the 20*mm* width of the copper plates, a plane stress element is used to simulate the solder joint and a plane strain element is used to simulate the copper plate. This simulation is more refined than a previous simulation (Ye et al. 2002b) in which both the solder joint and the copper plates were simulated with plane strain elements. Both ends of the copper plates are fixed to simulate the boundary conditions of the module in the fixture. An elastic material model is used for the solder. We realize that this is a gross assumption, but our aim here is to get a first order estimate of strains due to thermal loading. The material parameters for both solder and copper are shown in Table 7. The simulated distributions of strains are shown in Figures 49-50.

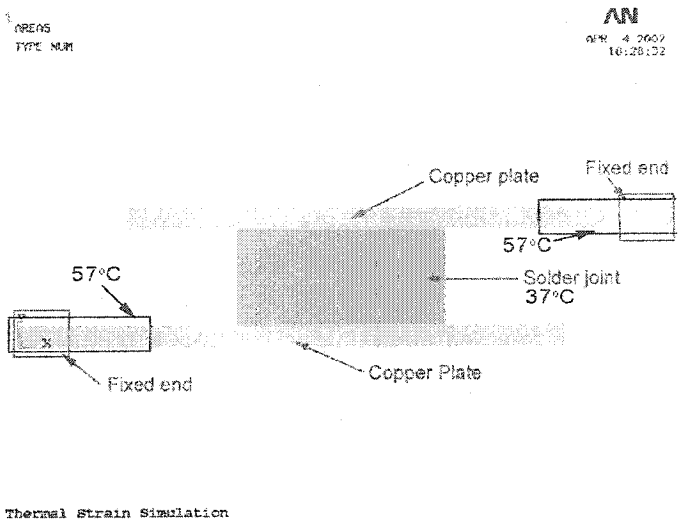


Figure 48 Geometry and boundary conditions used in FEM simulation

Table 7 Material parameters

Solder (Chandaroy 1998) (T is in *Kelvin*)	Copper
$E = 62 - 0.06TGPa$	$E = 117.2GPa$
$G = 24.3 - 0.029TGPa$	$\nu = 0.33$
$\alpha_T = 21.6\times10^{-6}/K$	$\alpha_T = 16.6\times10^{-6}/K$

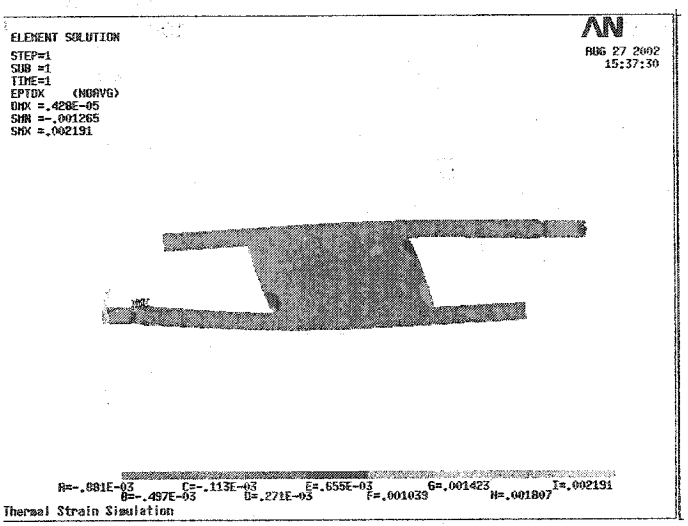


Figure 49 Simulated ε_x distribution

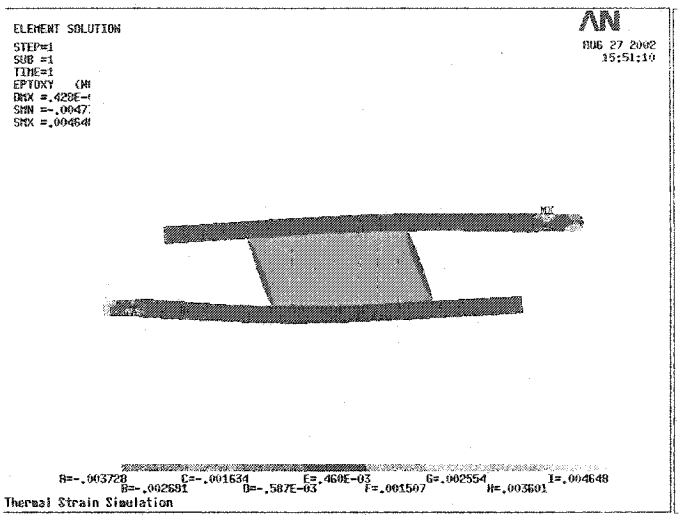


Figure 50 Simulated γ_{xy} distribution

4.1.5 Experimental and Simulation Comparison

Moiré interferometry fringes give the information of relative in-plane displacement. The Moiré interferometry fringes in the U and V fields represent isopleths of relative horizontal and vertical displacement, respectively. Since the strain fields are the gradient fields of the displacement fields, numerical differentiation is needed to extract strain from experimental fringe measurements. A natural cubic spline interpolation method is used to improve the results of this numerical process. This numerical differentiation process generally gives good accuracy for strains extracted from the fringe measurement when the data points for interpolation are sufficient. When there very few data points (indicating small variation of displacements in the x or y direction, but not necessary small strains) are available for interpolation, a loss of accuracy of an order of magnitude in numerical differentiation is possible (Post et al. 1994).

When calculating the shear strain from the Moiré interferometry fringes, as shown in Figures 40-41 (e.g. the gradient of vertical displacement along the x (horizontal) direction or horizontal displacement along the y (vertical) direction), the differentiation

accuracy is good due to the high density data. Figures 51 and 52 give the distribution of shear strain γ_{xy} along Line 3 (Figure 44) for both experimental (after 1h:40m) and simulated results due to thermal stressing, and the numbers are in very close agreement.

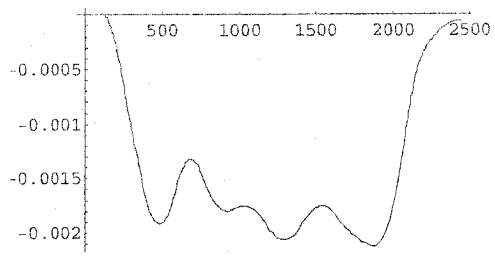


Figure 51 Shear Strain γ_{xy} distribution along Line 3 from Moiré Interferometry Measurements (horizontal coordinate in *nm*)

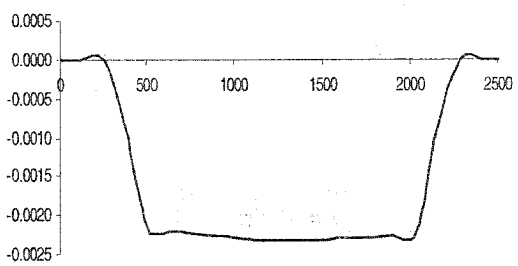


Figure 52 Shear Strain γ_{xy} distribution along Line 3 from FEM simulation (horizontal coordinate in *nm*)

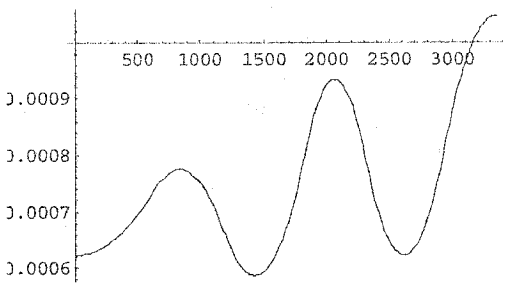


Figure 53 Normal Strain ε_x distribution along Line 1 from Moiré Interferometry Measurements (horizontal coordinate in *nm*)

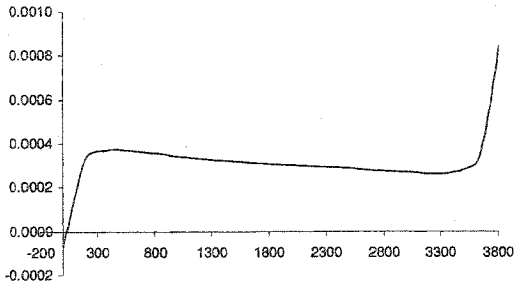


Figure 54 Normal strain ε_x distribution along Line 1 from FEM simulation (horizontal coordinate in *nm*)

Figure 53 and Figure 54 show the distribution of normal strain ε_x along the Line 1 (Figure 44) for both experimental (after 1h:40m) and simulated results. The experimental and simulated results both indicate that the normal strain ε_x is mostly in expansion and at the order of 10^{-3}. Figures 55-56 give the distributions of strain ε_y along the Line 3 for both experimental (after 1h:40m) and simulated results. Both the refined FEM simulation and experimental results indicate that strain ε_y is in expansion in the regions of the copper plates and in compression in the solder region.

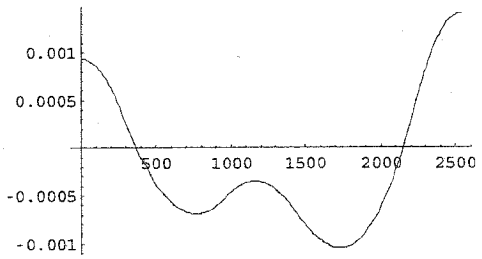


Figure 55 Transverse Strain ε_y distribution along Line 3 from Moiré Interferometry Measurements (horizontal coordinate in *nm*)

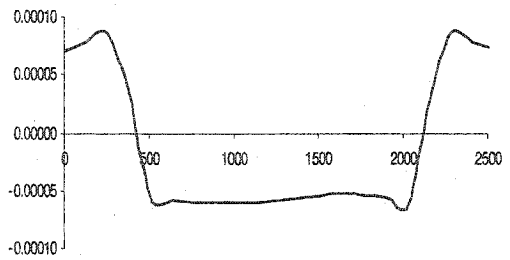


Figure 56 Transverse Strain ε_y distribution along Line 3 from FEM simulation (horizontal coordinate in *nm*)

However, the strain ε_y calculated from experimental fringes is over 10 times greater than that predicted by simulation. Such discrepancy is attributed to the numerical differentiation from the Moiré interferometry fringes. Since ε_y is the gradient ($\varepsilon_y = \frac{\partial V}{\partial y}$) along y and there are few Moiré interferometry fringes, poor numerical differentiation occurs. Though the measured value of ε_y is not highly accurate, the tendency of Moiré interferometry fringes to change direction is observable, and indicates a change of sign for the strain along the vertical line. This difference could also be due to viscoplastic response of solder alloys and small contribution of current stressing.

The results of this testing and refined FEM simulation strongly suggests that the strains observed in the experiment are largely due to thermal stressing and only minimally due to current stressing at the current density used thus far. This is because the Moiré interferometry experimental results closely resemble the finite element simulation where the only loading is temperature change. If the effect of electric current is dominant, the experimental results should deviate greatly from the simulation where only thermal stressing is considered. The agreement between the experiment and FEM simulation supports the use of Moiré Interferometry as a reliable approach in measuring in-situ displacement of BGA solder joints under current stressing.

4.1.6 Discussion

In this section, displacement evolution in a BGA solder joint under electrical current stressing was monitored in real time with Moiré Interferometry as the first step in building a constitutive model for solder material under current stressing. A FEM simulation of thermal stressing was performed which exhibited good agreement with Moiré Interferometry results. Moiré Interferometry is a reliable technique to measure in-situ displacement of BGA solder joints under current stressing. The results of this testing and refined FEM simulation strongly suggest that the strains observed in the first experiment are largely due to thermal stressing and only minimally due to current stressing at low current density.

4.2 Testing of Lead-free BGA Solder Joint with Improved Thermal Management

As shown in the preliminary Moiré Interferometry experiment, thermal deformation due to joule heating can be dominant if the contact resistance is not well managed. Improved test sample and test fixture schemes are introduced in the following experiments, which greatly reduce the contact electrical resistance and joule heating during current stressing. Lead-free solder joints are used in these experiments. The reason for choosing lead-free solder in the later experiments is the industrial tendency of eliminating lead in the solder due to environmental concerns.

In the following Moiré Interferometry experiments, the temperature was well controlled. This is done by applying a larger clamping force so that the close electric contact between the test vehicle and fixture is maintained; therefore excessive joule heating at the contact interface is greatly reduced as will be described in detail in section

4.2.1. A small fan is used to further reduce the temperature of the test vehicle during the electric current stressing. Lead-free solder (SnAg4Cu0.5) was used to fabricate the test module. On each test module there are two solder joints. One solder joint has been purposely made much bigger than the other one (Figure 57). Only the smaller solder joint on the test module was replicated with diffraction grating and was measured with Moiré Interferometry during electric current stressing. 4 modules were tested. The tested solder joints have different width and thickness and are thus subjected to different current densities. Due to the better thermal management in the new experiments, much higher current density was applied to the solder joint without much heat generation. The test modules are named as M-Pbfree-1, M-Pbfree-2 …, etc.

4.2.1 New Test Sample and Fixture Schemes

In the previous experiment, the temperature during current stressing at the interface of the copper plates of BGA module and the clamping fixture was much higher than that atop the copper plate. This indicates that the primary joule heating source was the interface between the copper plate and clamping fixture, where the electric contact resistance was high. Normally, the contact resistance can be reduced if greater clamping force is applied. However, the "Z" shape of the test module (Figure 32c) makes it difficult to apply high clamping pressure without creating large shear deformation in the solder joint (Figure 33b). This is because the height of the solder joint cannot be absolutely controlled during solder reflow. In order to solve this problem, new design of test module and fixture are introduced in the following experiments.

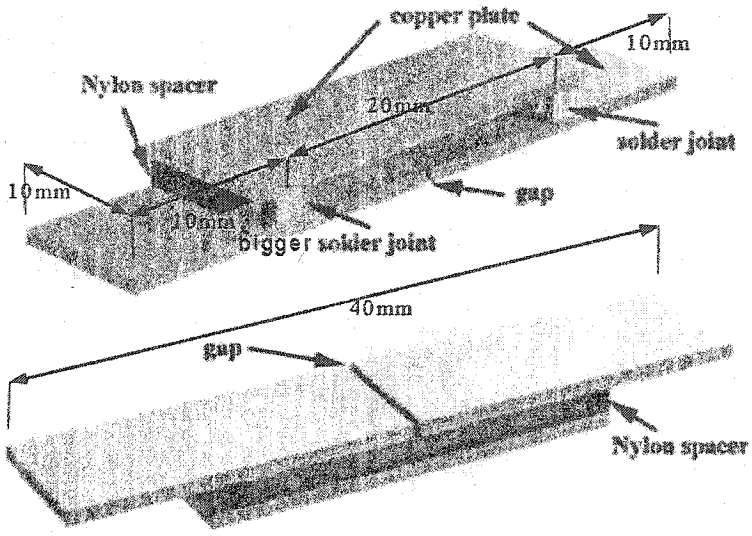


Figure 57 new scheme of the test BGA module

Figure 57 shows the new scheme of the test BGA module. The fabrication of the BGA module follows the same procedure as described in section 4.1.1. Instead of sectioning the test module into the shape as shown in Figure 32c, the test module is sectioned into the shape as shown in Figure 57. The thickness of the copper plate is increased to 0.6μm. A dielectric nylon spacer is glued between the upper and lower copper plates with epoxy to make the module less susceptible to mechanical deformation when higher clamping pressure is applied. There are two solder joints on the test module. A gap is sectioned in the lower copper plate to force the solder joints to carry the electric current (Figure 57). One solder joint is purposely made much bigger than the other so that electromigration is restricted in the smaller solder joint (it is also carefully polished to a very thin thickness), which carries much higher current density. The Moiré Interferometry experiment is only done on the smaller solder joint. The new scheme of test fixture is shown in Figure 58.

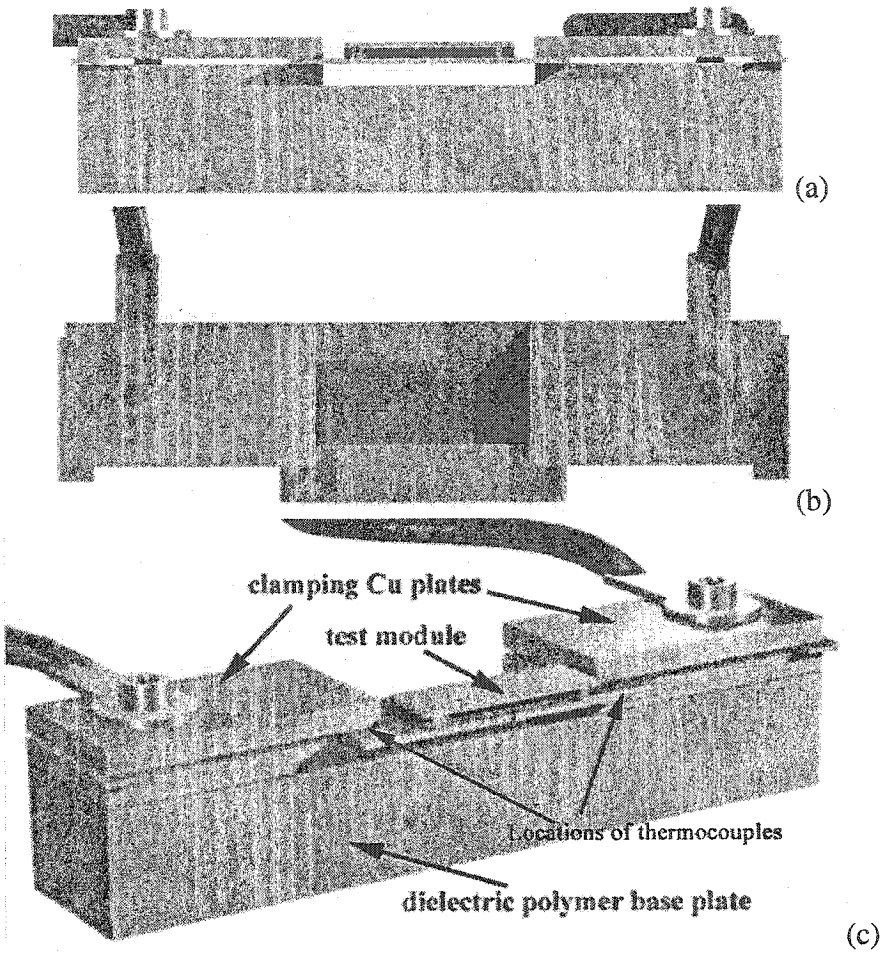


Figure 58 New scheme of the test vehicle fixture (a) front view (b) plane view (c) 3-D view

In the new test vehicle fixture, copper plates are used instead of steel plates to clamp the test module in order to reduce electric contact resistance. In the new design of test vehicle and fixture, much higher clamping pressure can be applied without introducing large deformations in the solder joint. It is shown in the following experiments that the electric contact resistance is greatly reduced with these new measures.

4.2.2 Moiré Interferometry Experiments on Lead-free Solder Joints

In module M-Pbfree-1, the smaller solder joint was polished to a thin section. The height of the solder joint was 1.5mm with an approximate width of 1.35mm. The joint was sectioned and polished to give an average thickness of about 0.25mm. In the experiment, 20 *Amps* of current was applied and a current density around 6000 A/cm^2 was achieved in the solder joint. In all the experiments, the current flow direction is controlled to be from upper copper plate downward to lower copper plate in the test solder joint. The temperature was kept almost constant at 26*°C*, as shown in Figure 59. There were some fluctuations (within 2°C) of temperature during current stressing. This was due to the ambient temperature fluctuation (considering the stressing takes several days or even months, in some cases) in the testing room which was central air conditioned. Thermocouple located at the clamping interface (Figure 58c) confirmed that the clamping interface did not have a higher temperature than that atop the copper plate of the test module. The effectiveness of the new test module and fixture design is clearly demonstrated by the fact that the temperature increase is much lower than that in the preliminary experiment even when much higher electric current was applied.

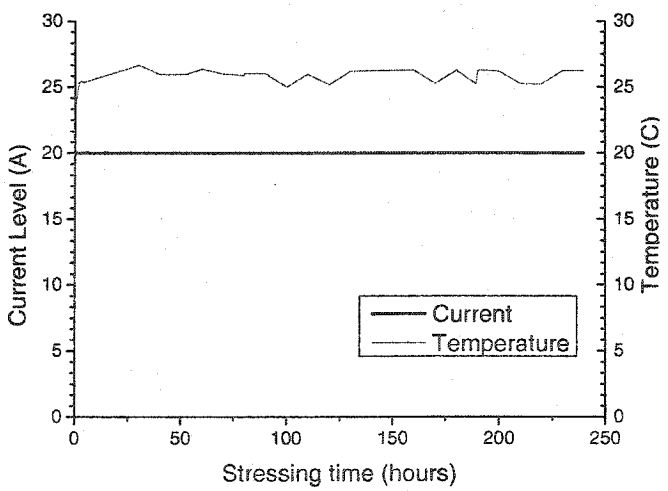
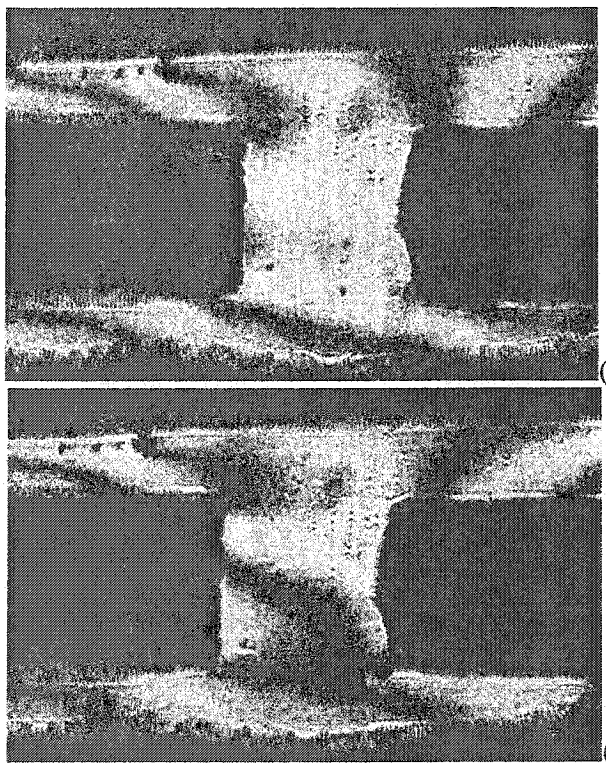


Figure 59 Profile of applied current and measured temperature history for M-Pbfree-1

The Moiré fringe evolution of module M-Pbfree-1 is shown in Figure 60 and Figure 61 for the *U* and *V* fields, respectively. Very few *U* and *V* field fringes developed after the solder joint was stressed for 240 hours. Both the U field fringes and V field fringes get denser with stressing time. The U field fringes stay near vertical and the V field fringes stay near horizontal. This result indicates there was little shear deformation, contrary to the previous experiment described in section 4.1.2. Since near constant temperature was maintained, it is appropriate to conclude that current stressing caused these displacements. If thermal stressing dominates electric current stressing, shear deformation is expected to be dominant, as in the previous experiment (and this was verified by the FE simulation).



(a)

(b)

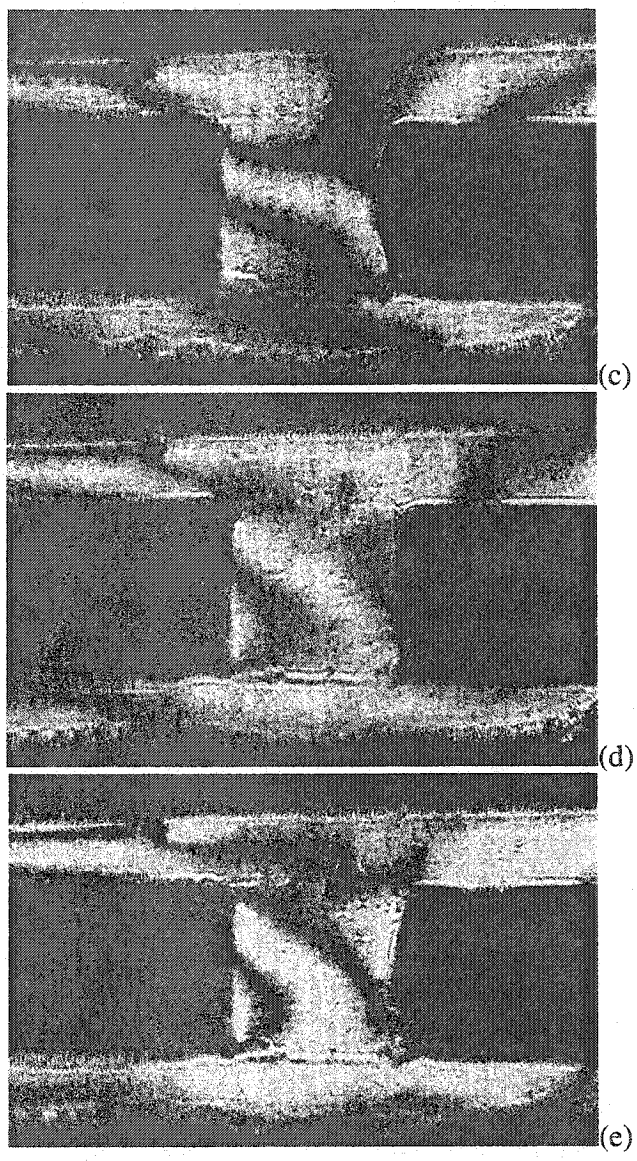
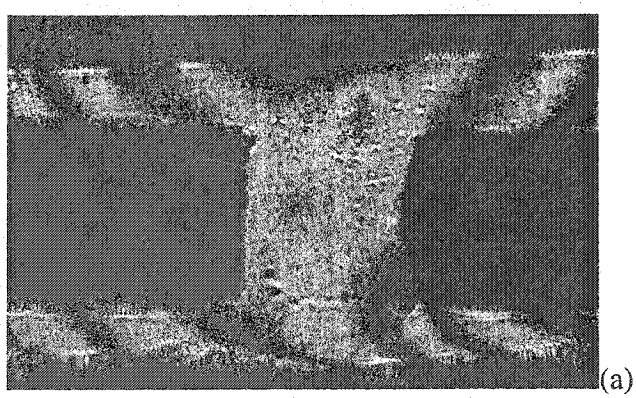


Figure 60 U field fringe evolution: module M-Pbfree-1 (a) initial (b) 66 hours (c) 115 hours (d) 190 hours (e) 239 hours



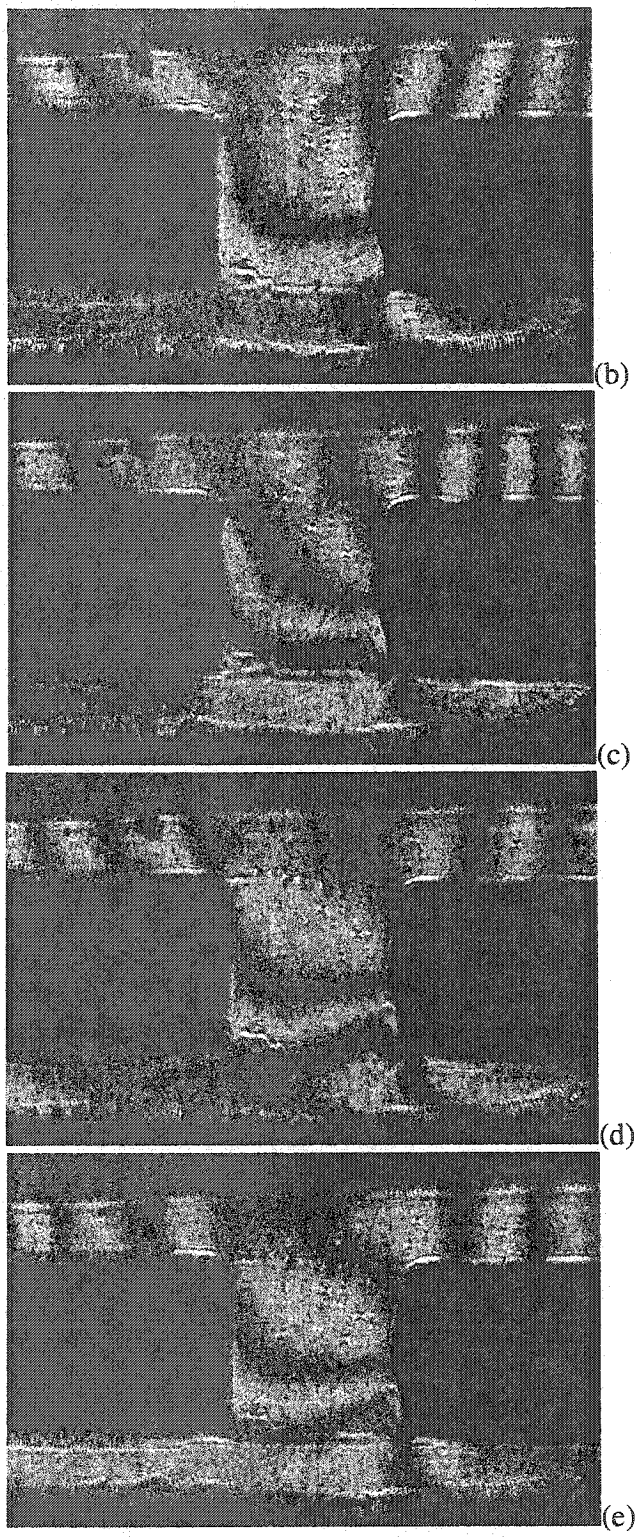


Figure 61 V field fringe evolution: module M-Pbfree-1 (a) initial (b) 66 hours (c) 115 hours (d) 190 hours (e) 239 hours

Similar experimental results were observed for module M-Pbfree-2. The height of the solder joint was 1.5mm with an approximate width of 1.35mm. The joint was sectioned and polished to give an average thickness of about 0.4mm. In the experiment, 29 *Amps* of current was applied and a current density around 5400 A/cm^2 was achieved in the solder joint. The temperature was kept almost constant at 27*°C*, as shown in Figure 62. There were some fluctuations of temperature (within 2°C) during current stressing. Thermocouple confirmed that the clamping interface did not have a higher temperature than that atop the copper plate of the test module.

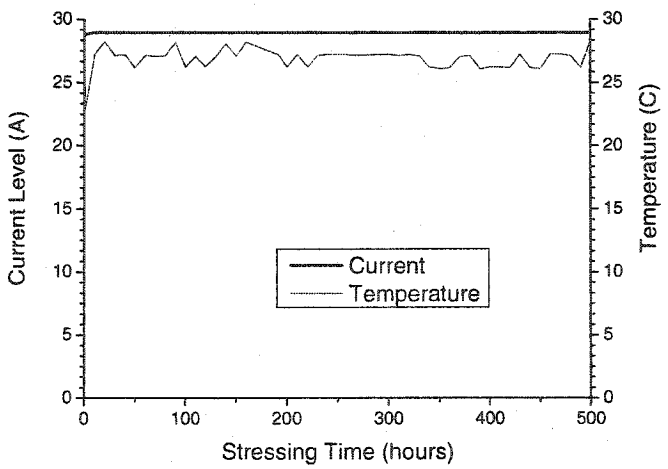
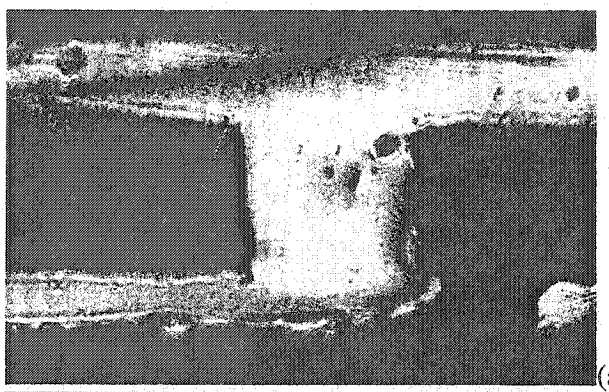
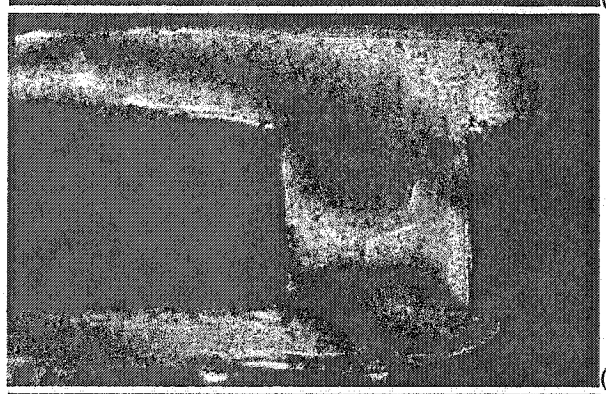


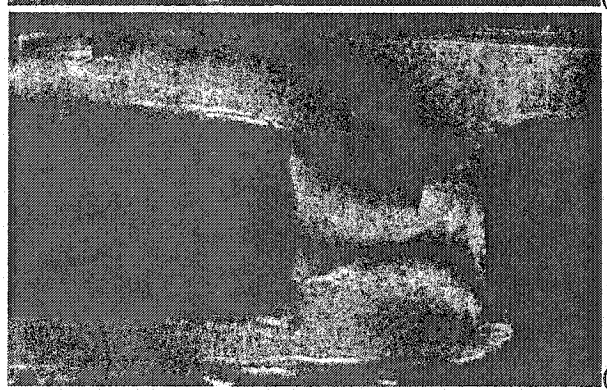
Figure 62 Profile of applied current and measured temperature history for M-Pbfree-2

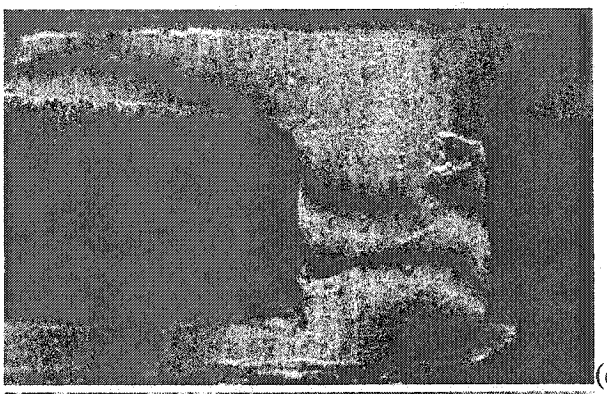
The Moiré fringe evolution of module M-Pbfree-2 is shown in Figure 63 and Figure 64 for the *U* and *V* fields, respectively. Very few *U* and *V* field fringes developed after the solder joint was stressed for an extensive 500 hours. Both the U field fringes and V field fringes get denser with stressing time. A couple of horizontal V field fringes indicate that there was a little shear deformation in the solder joint during the current stressing which came from the thermal expansion, but the shear deformation is not significant. In the V field, the fringes were horizontal, indicating some normal strain in the vertical direction developed during current stressing. The evolutions of fringes in both

fields were observed to be steady after 300 hours of current stressing; indicating the deformation of solder joint under electric current stressing enters steady state after 300 hours of stressing.


(a)


(b)


(c)


(d)

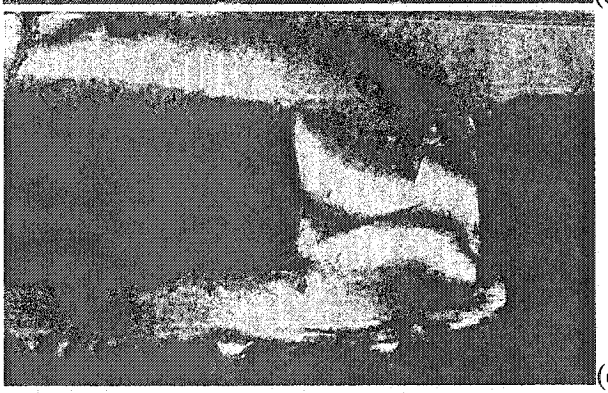
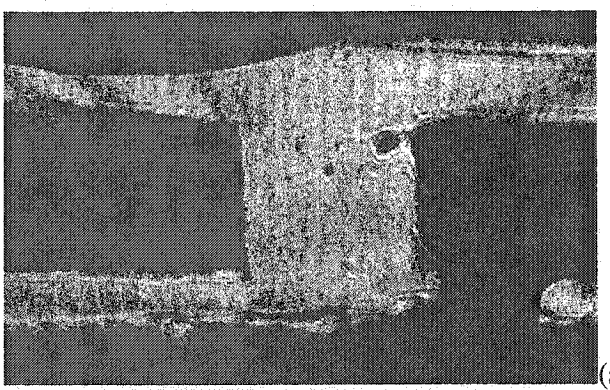
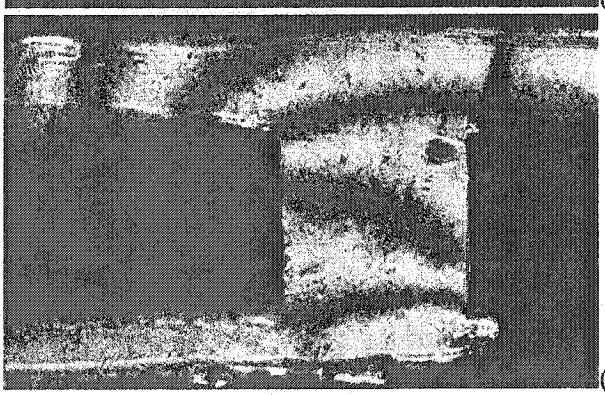

(e)

Figure 63 U field fringe evolution: module M-Pbfree-2 (a) initial (b) 97 hours (c) 170 hours (d) 266 hours (e) 505 hours


(a)


(b)

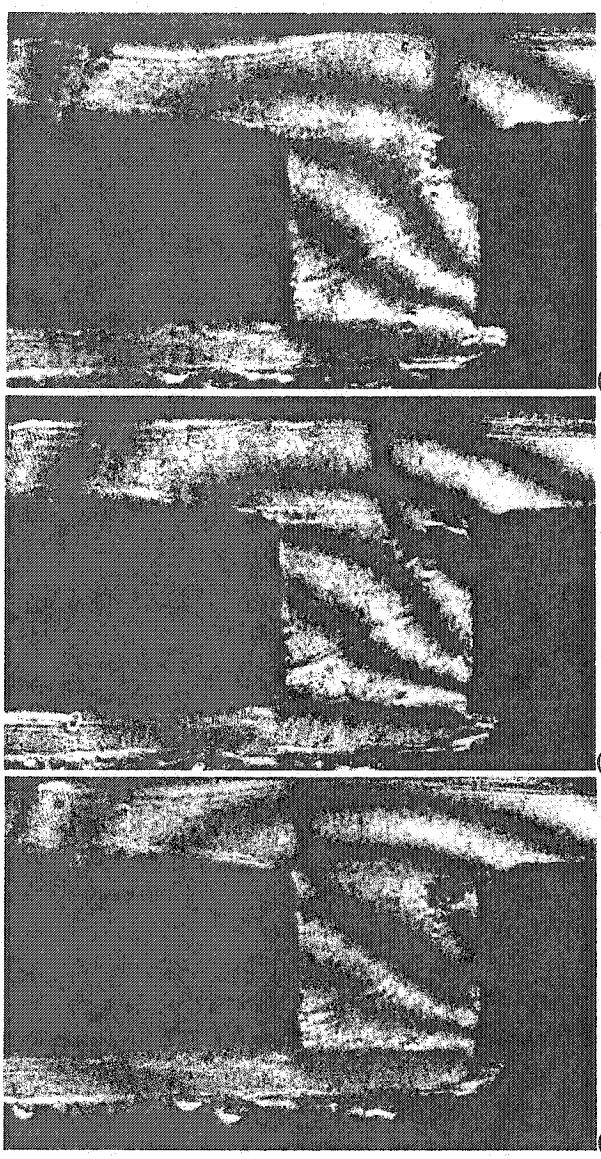


Figure 64 V field fringe evolution: module M-Pbfree-2 (a) initial (b) 97 hours (c) 170 hours (d) 266 hours (e) 505 hours

In the third experiment, we managed to make the test solder joint even smaller in order to achieve higher electric current density. In module M-Pbfree-3, the height of the solder joint is 1.5*mm* and the width is reduced to 1*mm*. The thickness of the solder joint is polished down to 0.25mm. In the experiment, 28 *Amps* of current was applied and a current density around 1.12×10^4 A/cm^2 was achieved in the solder joint. The temperature was kept almost constant at 29*°C* as shown in Figure 65. There were some fluctuations of

temperature (within 4°C) during current stressing (considering this experiment took over a month, the fluctuation is reasonable). Thermocouple confirmed that the clamping interface did not have a higher temperature than that atop the copper plate of the test module.

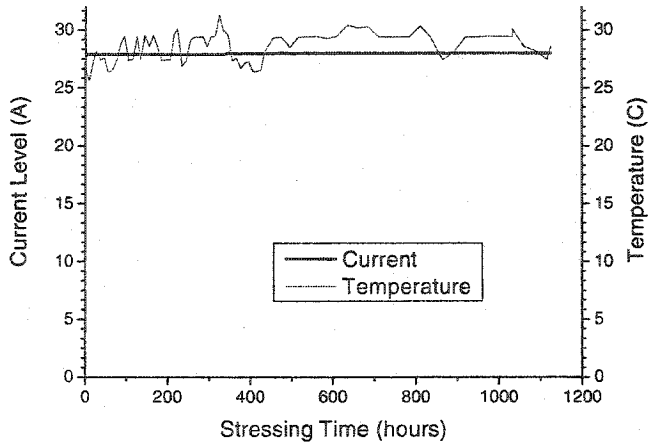


Figure 65 Profile of applied current and measured temperature history for M-Pbfree-3

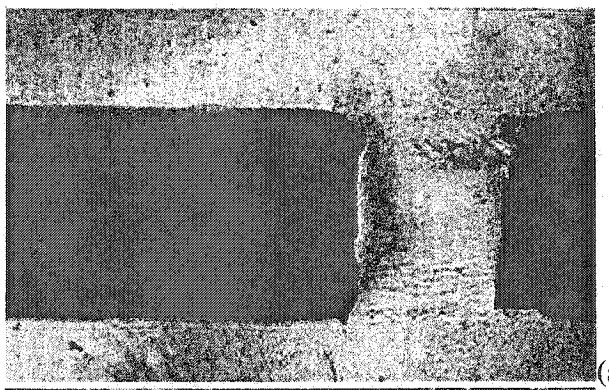
The Moiré fringe evolution of module M-Pbfree-3 is shown in Figure 66 and Figure 67 for the *U* and *V* fields, respectively. Unlike the experiments of M-Pbfree-1 and M-Pbfree-2, both U and V fields developed a lot of fringes during the course of current stressing. The U field fringes are predominantly in the vertical direction with concentrations on both vertical edges; indicating that large normal deformation developed in the horizontal direction but the horizontal normal deformation was not uniform along the height of the solder joint. A couple of horizontal fringes developed in the U field at the early stage of current stressing. This indicates that there was a little shear deformation due to thermal stressing (despite better thermal management, there was still a 5°C temperature increase during current stressing). The V field fringes are predominantly in the horizontal direction indicating a large transverse deformation in the vertical direction. The evolution of the fringes in both fields was observed to be steady after 1000 hours of

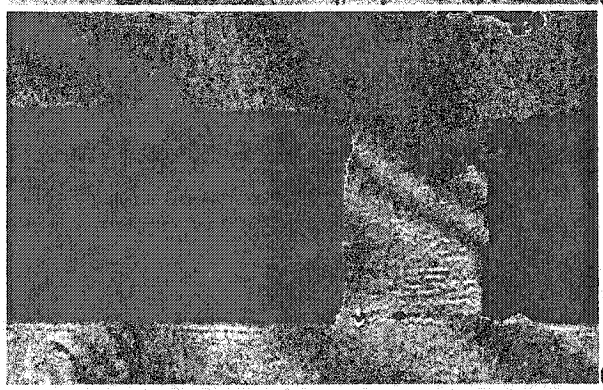
current stressing. This indicates that the deformation of solder joints under electric current stressing enters steady state after 1000 hours of stressing. Figure 66 and Figure 67 also clearly show that the quality of diffraction grating on the solder joint degraded substantially after 1000 hours of stressing. We think that this is due to the diffusion in the solder joint underneath the diffraction grating.

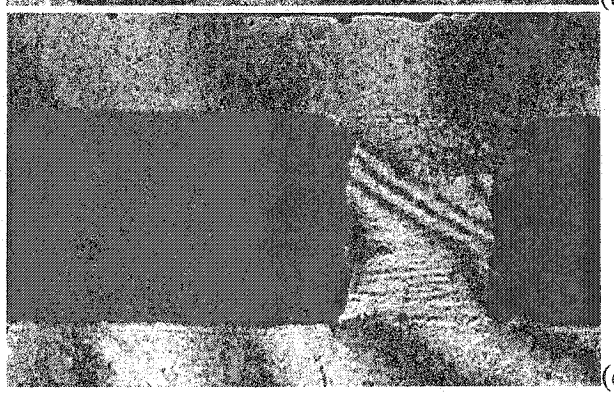
The dense fringes observed in module M-Pbfree-3 is fundamentally different in several ways from those observed in the preliminary experiment, as reported in section 4.1.2. First, in the preliminary experiment, the U field fringes are predominantly in the horizontal direction and V field fringes are predominantly in the vertical direction, which indicates that shear deformation was dominant in the solder joint. Whereas, there was only a little shear deformation in the solder joint of M-Pbfree-3 and normal deformations in both horizontal and vertical direction are dominant.

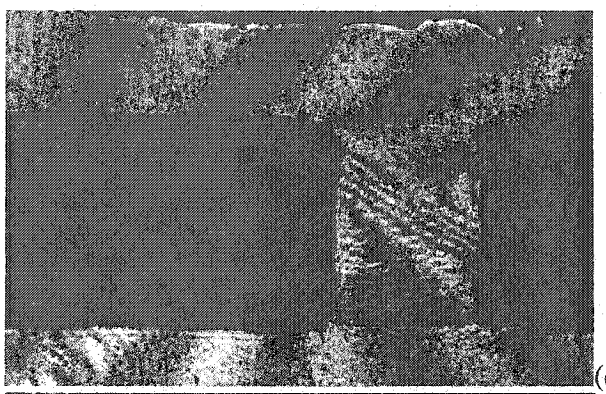
Second, there was a large temperature increase in the preliminary experiment (a 15°C increase atop of copper plate and a 35°C increase near the clamping interface), where the thermal expansion of the copper plates contributed to the observed shear deformation in the solder joint. This is verified by the FEM analysis in section 4.1.4. On the other hand, the temperature increase in M-Pbfree-3 (as well as in M-Pbfree-1 and M-Pbfree-2) was much lower and uniform across the whole test module. And the temperature was kept near constant for hundreds of hours of current stressing. Therefore, thermal deformation cannot account for the subsequent development of normal deformation during those hundreds of hours of current stressing. The resulting shear deformation from the thermal expansion was not significant.

Third, the fringe development in the preliminary experiment took only hours if not minutes, which is the time for heat to transfer; but the development of fringes in M-Pbfree-3 (as well as in M-Pbfree-1 and M-Pbfree-2) took hundreds of hours to reach steady state. Such a long development time can only be explained by the coupled mechanical-diffusional electromigration process. Based upon the above analysis, it is clear that the deformation fringes we observed in M-Pbfree-3 (as well as in M-Pbfree-1 and M-Pbfree-2) are mostly due to current stressing (electromigration).

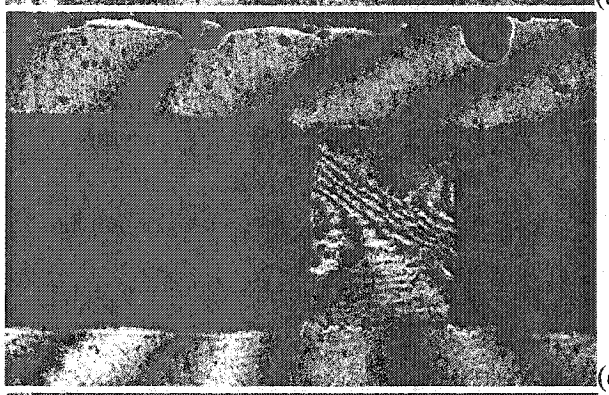

(a)


(b)


(c)



(d)



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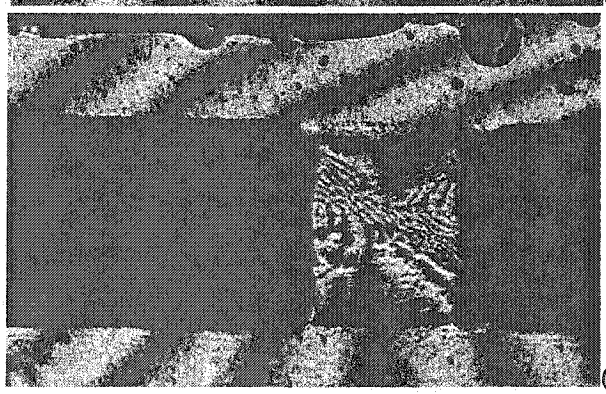
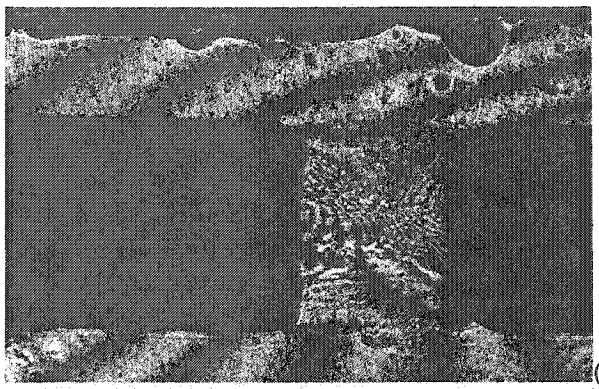
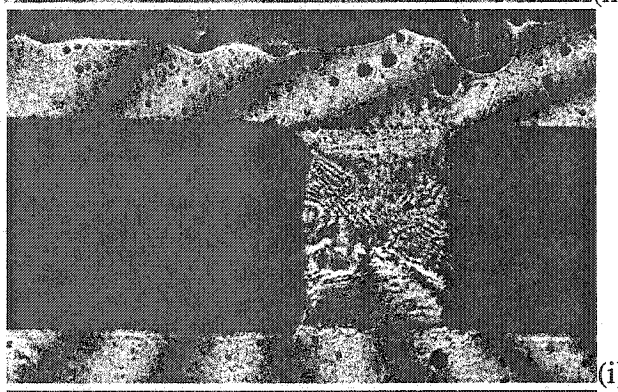


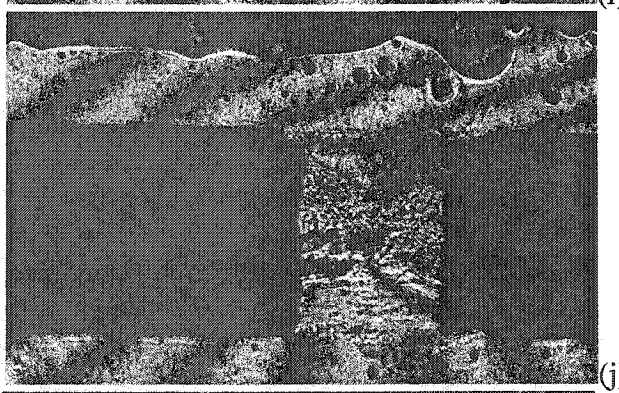
(g)



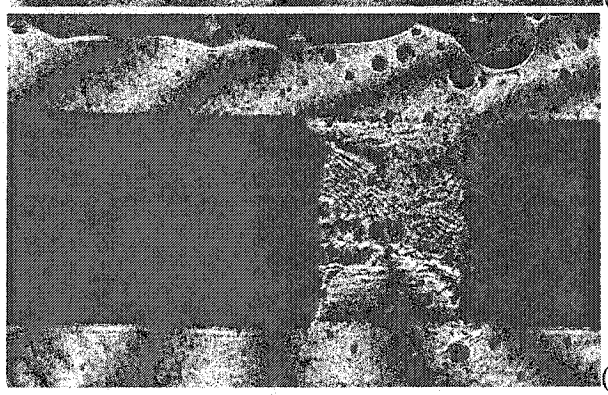
(h)



(i)



(j)



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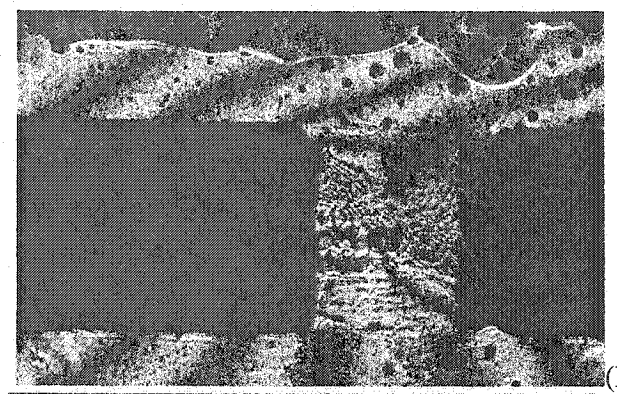

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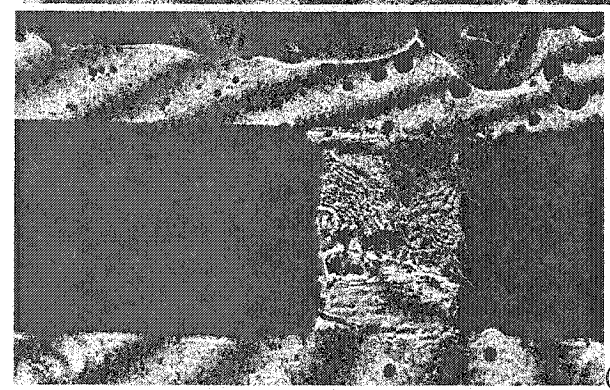
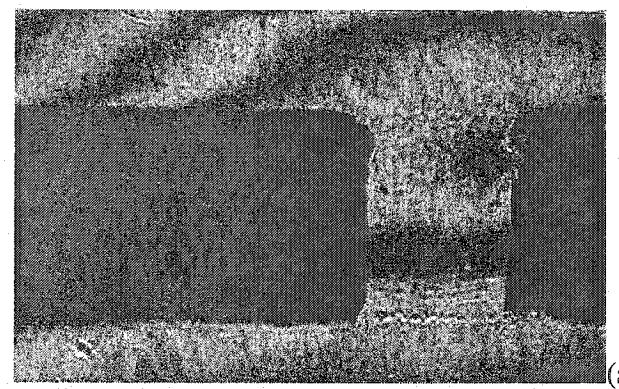
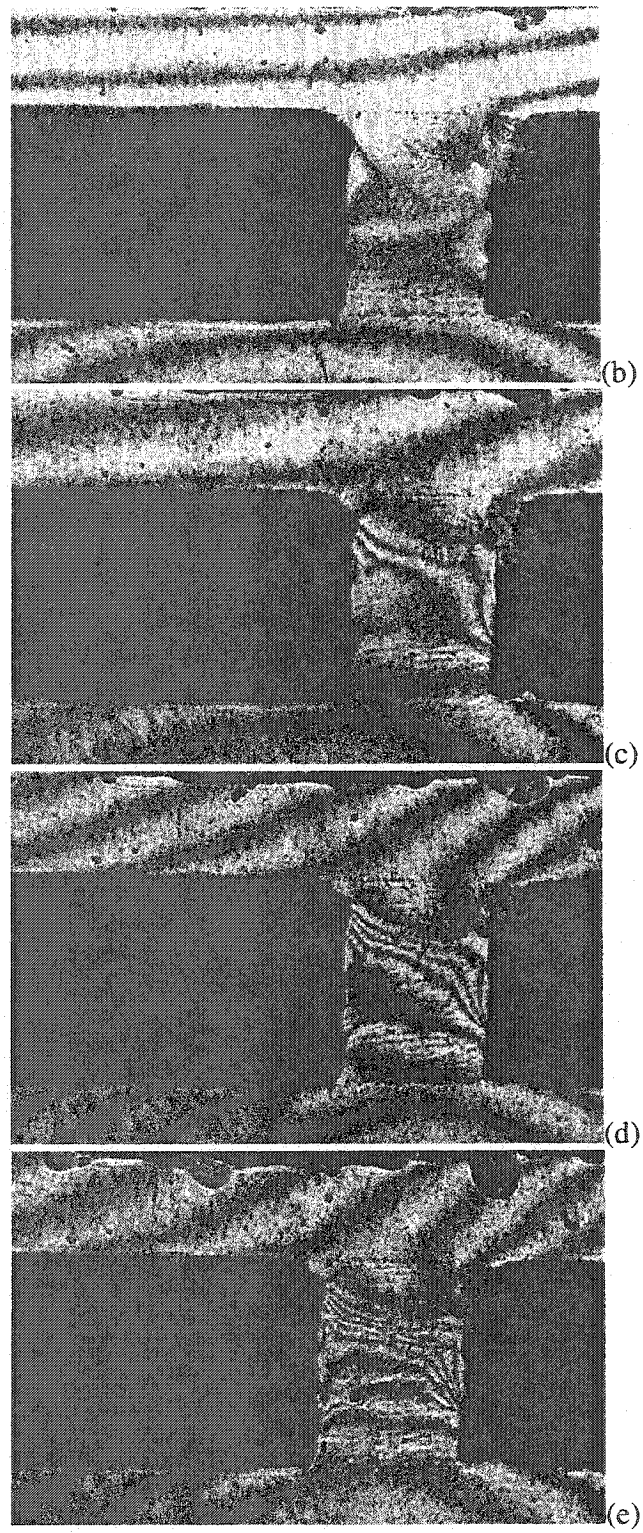


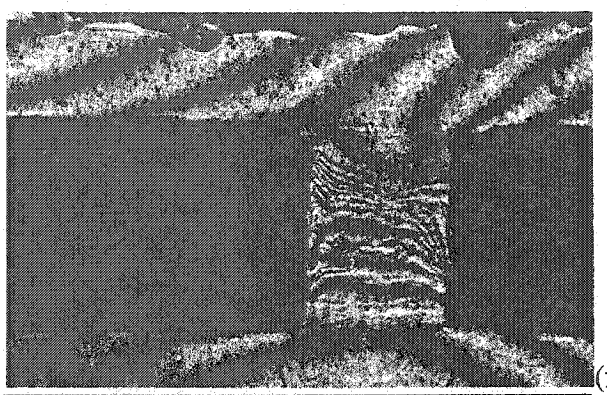
(m)

Figure 66 U field fringe evolution: module M-Pbfree-3 (a) initial (b) 125 hours (c) 189 hours (d) 292 hours (e) 390 hours (f) 482 hours (g) 556 hours (h) 645 hours (i) 765 hours (j) 839 hours (k) 935 hours (l) 1033 hours (m) 1125 hours

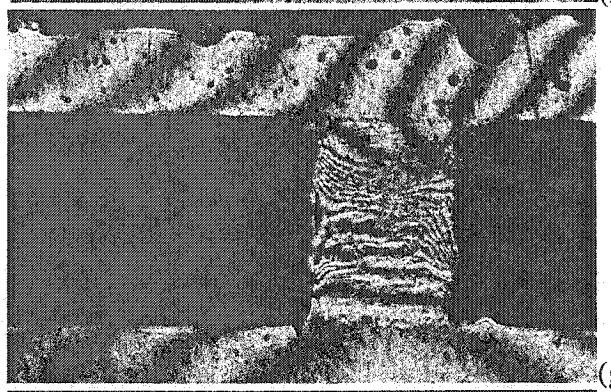


(a)





(f)



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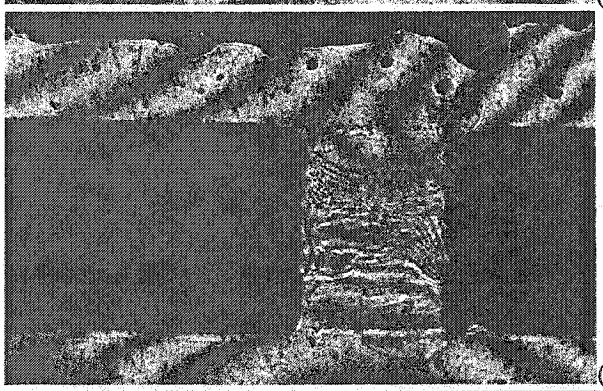
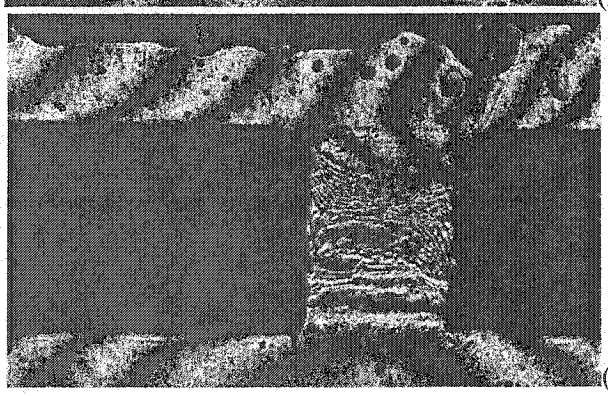


(h)



(i)

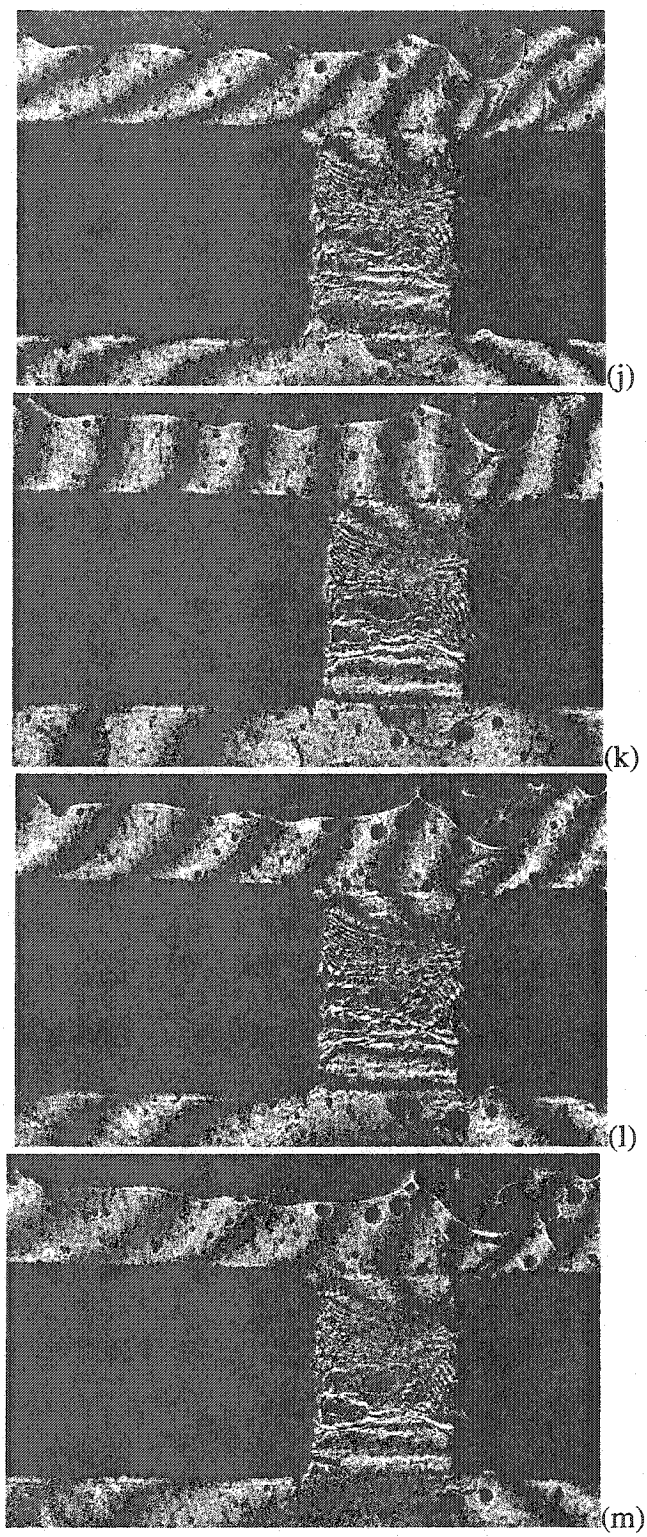


Figure 67 V field fringe evolution: module M-Pbfree-3 (a) initial (b) 125 hours (c) 189 hours (d) 292 hours (e) 390 hours (f) 482 hours (g) 556 hours (h) 645 hours (i) 765 hours (j) 839 hours (k) 935 hours (l) 1033 hours (m) 1125 hours

In the fourth experiment, we tried to make the current density even higher in the test solder joint. This was done by applying a higher electric current level of 40 *Amps*. In module M-Pbfree-4, the height of the solder joint is 1.5*mm* and the width is 1.2*mm*. The thickness of the solder joint is polished down to 0.25mm. In the experiment, 40 *Amps* of current was applied and a current density around 1.33×10^4 A/cm^2 was achieved in the solder joint. The temperature was kept almost constant at 30°C, as shown in Figure 68. There were some fluctuations of temperature (within 2°C) during current stressing. Thermocouple confirmed that the clamping interface did not have a higher temperature than that atop the copper plate of the test module.

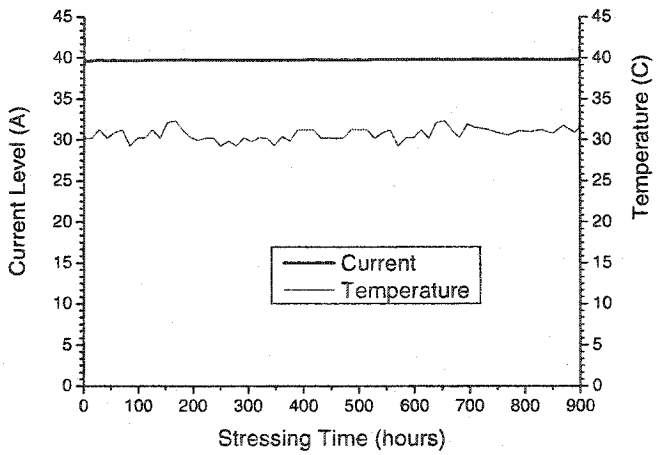
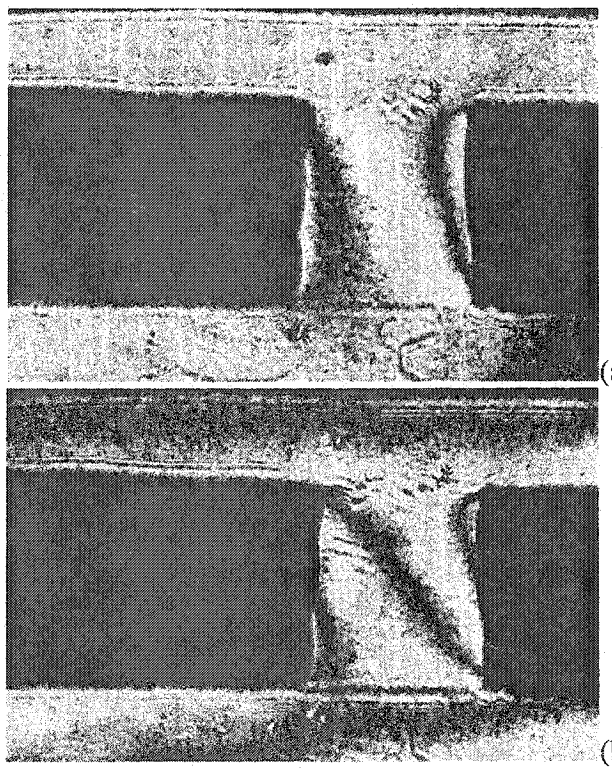


Figure 68 of applied current and measured temperature history for M-Pbfree-4

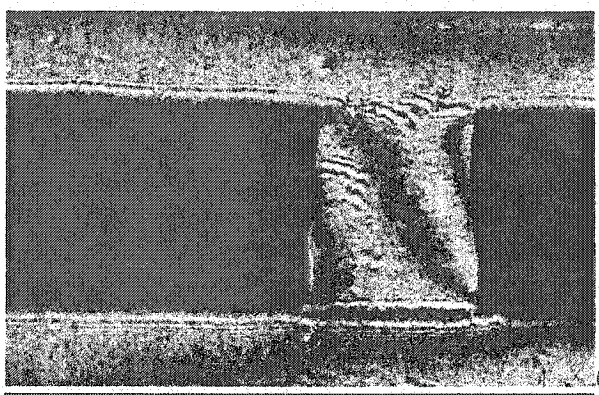
The Moiré fringe evolution of module M-Pbfree-4 is shown in Figure 69 and Figure 70 for the *U* and *V* fields, respectively. Since the average current density in the solder joint of M-Pbfree-4 is higher than that in M-Pbfree-3, it is reasonable to expect denser fringes in both U and V fields. But contrary to our expectation, far fewer fringes were observed in both fields after same numbers of hours of current stressing. Both the U field fringes and V field fringes grow with stressing time. The U field fringes stay near vertical and the V field fringes stay near horizontal. This tendency is the same as in the

previous experiments and confirms that electric stressing leads to normal deformation in both horizontal and vertical directions. It is clear that in M-Pbfree-4, shear or thermal deformation was not dominant. The observation of lesser than expected fringes in this solder joint indicates that current density is not the only factor that affects the fringe development. It is further discussed in the later section that current density distribution is also a factor. The evolution of the fringes in both fields was observed to be steady after 700 hours of current stressing. This indicates that the deformation of the solder joint under electric current stressing enters steady state after 700 hours of stressing.

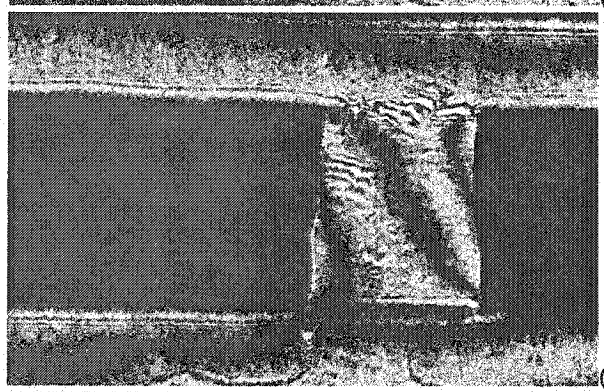


(a)

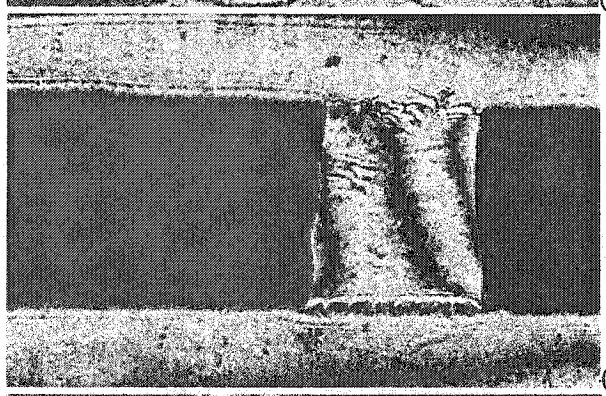
(b)



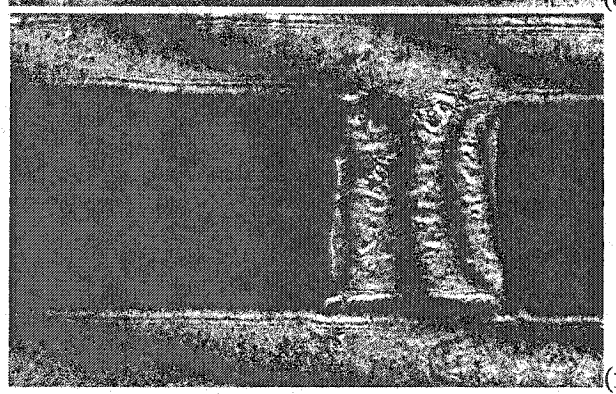
(c)



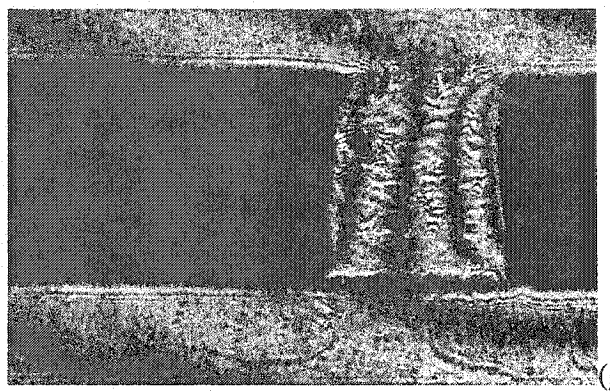
(d)



(e)

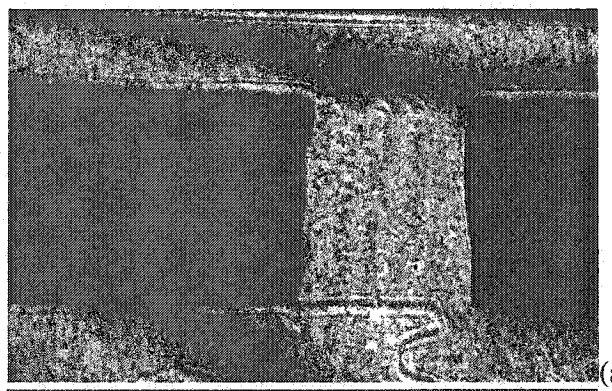


(f)

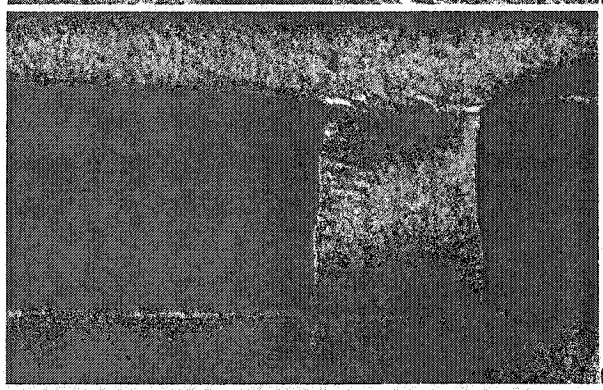


(g)

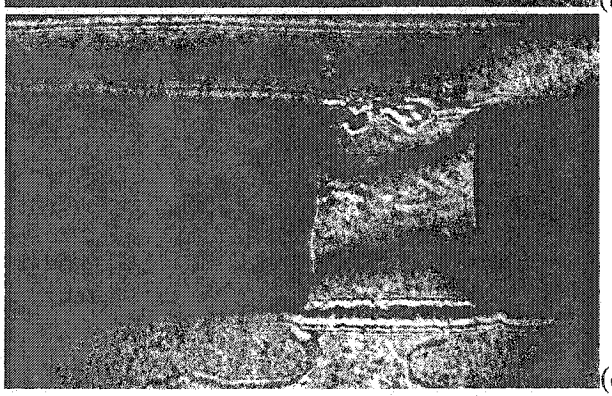
Figure 69 U field fringe evolution: module M-Pbfree-4 (a) initial (b) 75 hours (c) 263 hours (d) 380 hours (e) 500 hours (f) 690 hours (g) 879 hours



(a)



(b)



(c)

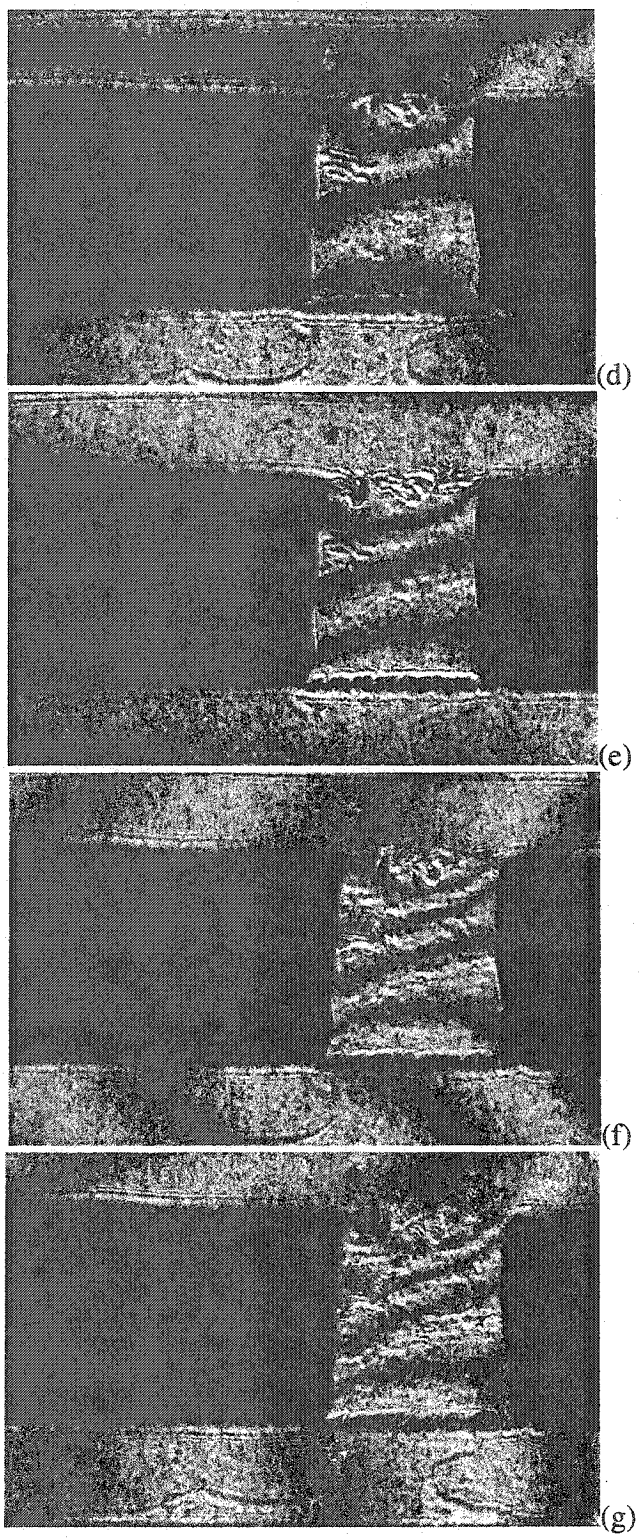


Figure 70 V field fringe evolution: module M-Pbfree-4 (a) initial (b) 75 hours (c) 263 hours (d) 380 hours (e) 500 hours (f) 690 hours (g) 879 hours

4.2.3 Irreversible Deformations in Solder Joint after Turning Current Off

In the current stressing experiment on module M-Pbfree-3, the solder joints were stressed under high current density for a total of 1500 hours. The deformation in the solder joint became unchanged after 1000 hours of current stressing as shown in the previous section. We kept recording the deformation fringes after the turning the electric current off.

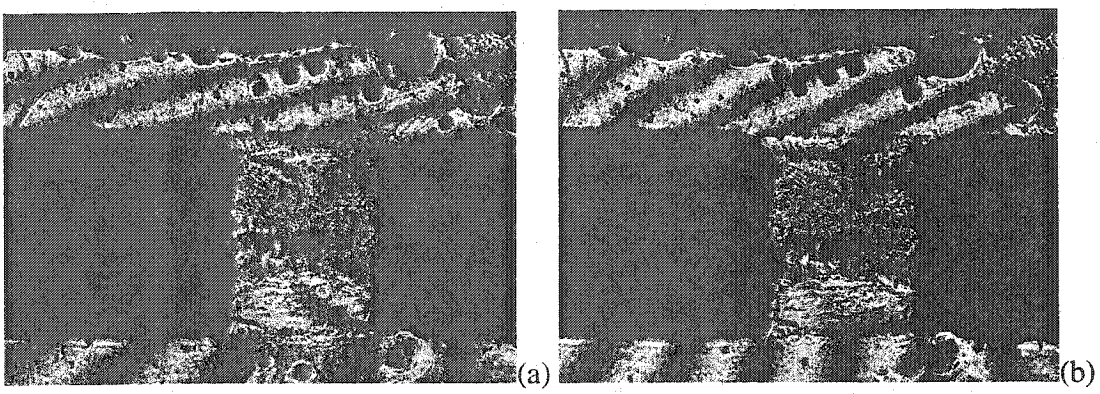


Figure 71 U field fringe of module M-Pbfree-3 (a) 1500 hours of current stressing (b) 72 hours after the current was turned off

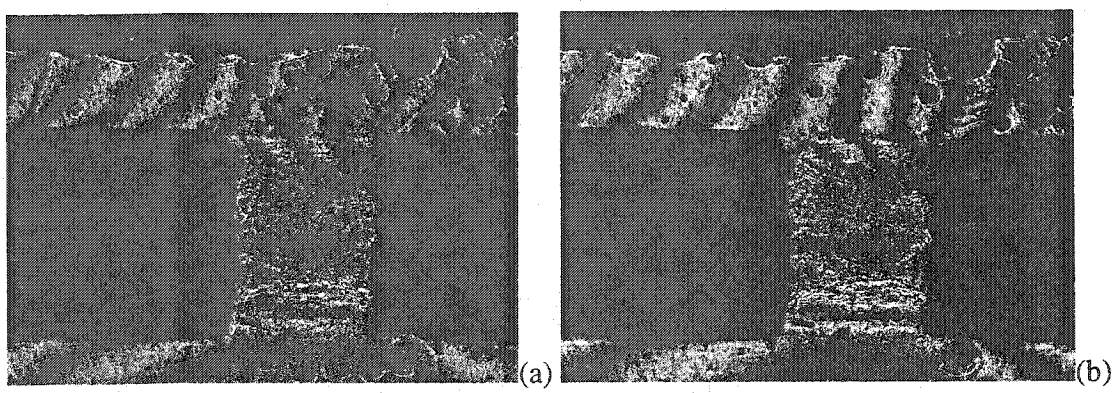


Figure 72 V field fringe of module M-Pbfree-3 (a) 1500 hours of current stressing (b) 72 hours after the current was turned off

Figure 71 and Figure 72 show the U field and V field fields fringes in the solder joint after 1500 hours of current stressing and 72 hours after the current was turned off. Although the fringes in the solder joint became less clear after 1500 hours of current stressing due to the degradation of diffraction grating, there were little changes in both U

and V field fringes after the current was turned off. This indicates that the deformations created by high current density are irreversible. However, these irreversible deformations are not the same as the plastic deformation. Plastic deformations are created by the high deviatoric (shear) stresses and correspond to the motion of large numbers of dislocations. The deformation created by electromigration is due to the re-arrangement of vacancies and atoms in the material as well as vacancy generations and annihilation due to diffusion and correspond to the volumetric strain at lattice site. However, as demonstrated in the numerical simulations, volumetric strain at lattice due to electromigration give rise to high level stresses that exceed the yield stress of the solder alloy, these high deviatoric stresses may create plastic deformations. Therefore, the irreversible deformations we observed in the experiments are the combination of electromigration deformations and plastic deformations.

4.2.4 Discussion

In this section, the Moiré Interferometry experimental results on four lead-free (SnAg4Cu0.5) solder joints under high electric current density stressing were reported. During electric current stressing, the stressing temperature on the test module was well controlled and almost held constant during the course of current stressing. This is done by applying a greater clamping force so that the close electric contact between the test vehicle and fixture is maintained. Therefore, excessive joule heating at the contact interface is greatly reduced, as was described in detail in section 4.2.1.

The current densities applied in these solder joints range from $0.5\sim1.33\times10^{4}A/cm^{2}$. This current density is much higher than that applied in the preliminary experiment. Since the temperature was held almost constant, the deformation fringes observed during

current stressing can only be attributed to current stressing. It was found that high current density stressing primarily induced normal deformations within the solder joints in the test modules, which are different from the primary shear deformations that induced by thermal stressing in the preliminary experiment. The deformations induced by current stressing were found to take hundreds of hours to reach steady state, which is consistent with the fact that electromigration took hundreds of hours to reach steady state. It also indicates that current density is not the only factor that affects the deformation development within the solder joint in the test modules. It is further discussed in the later section that current density distribution is also a factor.

4.3 Numerical Simulations and Discussions on the Deformation of Solder Joint under Current Stressing.

In Section 4.2, the deformation of lead-free solder joints under high electric current stressing is measured with Moiré Interferometry technique. The purpose of the experiment is to find the constitutive model of solder alloy under current stressing. The electromigration constitutive model presented in Chapter 3 is used to model the behavior of lead-free solder alloy under current stressing in this chapter. The numerical simulation results are compared to the experimental results.

4.3.1 Electromigration Constitutive Model Re-visited

Electromigration is viewed as a coupled diffusion-mechanical process in this study. The electron flow assisted vacancy diffusion process gives rise to volumetric strain at lattice site in the conducting solder alloy. Under the mechanical boundary constrains, the volumetric strain at lattice site due to diffusion results in stress build-up within the

structure. If the spherical stress state within the conducting solder is changed, or there is a spherical stress gradient created, the stress state will affect the vacancy flux or vacancy generation rate in the diffusion process. This coupled process is described by the following PDE system.

The vacancy diffusion equation of electromigration given by Kirchheim is (Kirchheim 1992):

$$\frac{\partial C_v}{\partial t} = -\vec{\nabla} \cdot \vec{q} + G \tag{4.2}$$

and $$\vec{q} = -D_v[\vec{\nabla} C_v + \frac{C_v Z^* e}{kT}(-\rho \vec{j}) - \frac{C_v}{kT}(-f\Omega)\vec{\nabla}\sigma]$$

This diffusion equation is sufficient to describe the tests that are reported in the previous section, where there is no significant temperature gradient in the solder joint. However, in the flip-chip solder joints which are subjected to high current density, a significant thermal gradient (up to several thousand degree C per centimeter) may be maintained due to joule heating in the silicon chip. This high thermal gradient can cause another biased mass diffusion in the direction of thermal gradient in solder joint, which is referred to as thermomigration. We will discuss the observation of thermomigration in flip-chip solder joints under high current density in Chapter 5. Assume the diffusion is by vacancy mechanism. The vacancy diffusion flux due to thermal gradient given by Huntington is (Huntington 1972):

$$\vec{q}_{th} = -\frac{D_v C_v}{kT^2} Q^* \vec{\nabla} T \tag{4.3}$$

where Q^* is the heat of transport for vacancy. Therefore, the total vacancy flux including thermomigration is then:

$$\vec{q} = -D_v[\nabla^2 C_v - \frac{Z^* e\rho}{kT}\vec{\nabla}\cdot(C_v\vec{j}) + \frac{C_v}{kT^2}Q^*\vec{\nabla}T + \frac{f\Omega}{kT}\vec{\nabla}\cdot(C_v\vec{\nabla}\sigma)] \qquad (4.4)$$

Combining these equations, we get the vacancy continuity equation:

$$\frac{\partial C_v}{\partial t} = D_v[\nabla^2 C_v - \frac{Z^* e\rho}{kT}\vec{\nabla}\cdot(C_v\vec{j}) + \frac{C_v}{kT^2}Q^*\vec{\nabla}T + \frac{f\Omega}{kT}\vec{\nabla}\cdot(C_v\vec{\nabla}\sigma)] + G \qquad (4.5)$$

The volumetric strain at lattice site due to vacancy diffusion and vacancy generation (Sarychev and Zhinikov 1999):

$$\dot{\varepsilon}_{ij}^{elec} = \dot{\varepsilon}_{ij}^{m} + \dot{\varepsilon}_{ij}^{g} = \frac{\Omega}{3}[f\vec{\nabla}\cdot\vec{q} + (1-f)G]\delta_{ij} \qquad (4.6)$$

The total strain tensor in the solder alloy is then the superposition of mechanical, thermal, and electromigration strains:

$$\varepsilon_{ij}^{total} = \varepsilon_{ij}^{mech} + \varepsilon_{ij}^{therm} + \varepsilon_{ij}^{elec} \qquad (4.7)$$

And the quasi-static mechanical equilibrium equation is:

$$\frac{\partial \sigma_{ij}}{\partial x_j} = 0 \qquad (4.8)$$

where σ_{ij} is the stress tensor; x_j is jth coordinate. The coupled diffusion-mechanical process can be model by solving the PDE system of Equations (4.5), (4.6), and (4.8). Other symbols in these equations which are not explained here are the same as those described in Chapter 3.

In the following simulations, only the elastic constitutive model is employed since the primary purpose of the simulation is to verify the electromigration constitutive model. But since no elastic stress-strain relationship is assumed in this model, more realistic constitutive model can be employed in this model in the future. Also as mentioned above, although the vacancy continuity Equation (4.5) includes the term of thermomigration, it

has no effect in our simulation, since there is only very small thermal gradient in the solder joints that were tested in the Moiré Interferometry experiments.

4.3.2 Model Parameters for Lead-Free Solder Alloy

The lead-free solder alloy used in the Moiré Interferometry experiment is Sn95.5/Ag4/Cu0.5. The melting point of this lead-free solder alloy is 218°C. Sn/Ag/Cu alloy has better reliability properties than Sn/Ag alloy. The biggest problem with Sn/Ag solder alloy is that different metallurgical phase structures may be formed in different areas within a solder joint when the cooling rate is different in these areas.. Therefore, Sn95.5/Ag4/Cu0.5 solder alloy is used in our experiments as the candidate for lead-free solder alloy.

In order to numerically simulate the deformation of the lead-free solder joint under electric current stressing, one needs to identify the material parameters to be used in the constitutive model. There was little work done on the diffusion properties of lead-free solder alloy, but there has been some diffusion and electromigration research work done on pure tin. Since the lead-free solder alloy used in this experiment contains 95.5% tin, the material properties of tin are taken in the numerical simulation as a first order approximation.

A. Equilibrium Vacancy Concentration

The atomic volume, Ω, of tin is $16.3 cm^3/mol$ or $2.71\times10^{-23} cm^3/atom$. The atomic concentration, C_a, of tin is $3.69\times10^{22}/cm^3$. The equilibrium vacancy concentration at a stress free state is reported as $C_{v0}/C_a = 3\times10^{-5}$ by Balzer and Sigvaldason (Balzer and Sigvaldason 1979), or $C_{v0}=1.11\times10^{18}/cm^3$.

B. Vacancy Diffusivity

Some research has been done on the diffusion and electromigration experiments of pure tin. Lange and Bergner (Lange and Bergner 1962) measured the self-diffusion along grain boundaries in polycrystalline Sn (99.99%) between 40 and 115°C. Sun & Orhring (Sun and Ohring 1976) developed a tracer-scanning technique to study self-diffusion and electromigration in evaporated thin Sn films at 142~213°C. Singh & Ohring (Singh and Ohring 1984) conducted the self-diffusion and electromigration experiment in evaporated thin Sn films at -50 to +198°C. Their grain boundary diffusivity measurements in pure tin are shown in Figure 73. The Lange & Bergner measurement agrees closely with that of Singh & Ohring's.

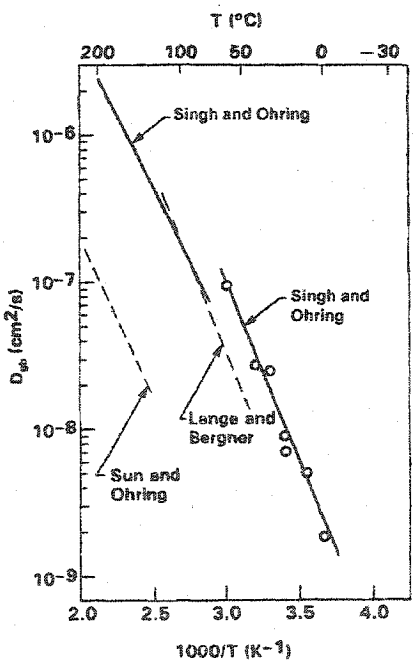


Figure 73 Summary of D_{gb} values in Sn (after Singh & Ohring (Singh and Ohring 1984))

The Singh & Ohring grain boundary diffusivity is found (Singh and Ohring 1984) by assuming a grain boundary width of 0.5nm:

$$D_{gb} = (4.9^{+15.6}_{-3.7})\exp[-(11700 \pm 840 cal/mol)/RT]cm^2/s \qquad (4.9)$$

where R = 8.3145J/mol=1.987cal/mol, is gas constant, and T is absolute temperature. In this simulation, the grain boundary diffusion is assumed to be the main diffusion mechanism in electromigration. By assuming an average grain size of d=300nm (Singh and Ohring 1984), the effective atomic diffusivity is thus:

$$D_a = \frac{\delta}{d} D_{gb} = \frac{0.5nm}{300nm} \times 4.9 \times \exp(-11700cal/RT) cm^2/s \qquad (4.10)$$

At 303K (30°C), D_a is calculated to be $2.97\times10^{-11} cm^2/s$. The vacancy diffusivity is calculated from the relation (Clement and Thompson 1995), $D_aC_a=D_vC_v$, at the stress free state. By assuming $C_{v0}/C_a = 3\times10^{-5}$ (Balzer and Sigvaldason 1979), $D_v=D_a/(3\times10^{-5})=1\times10^{-6} cm^2/s$ is derived and used in the following simulations.

C. Effective Charge Number Z^*

Lodding (Lodding 1965) and Kuz'menko (Kuz'menko 1962) reported the effective charge number Z^* values of pure tin ranging from -80 to -160. Sun & Ohring reported similar values (Sun and Ohring 1976). However, Khosla & Huntington (Khosla and Huntington 1975) reported effective charge number ranging from -10 to -16 in single-crystalline Sn and -12 in polycrystalline at temperature in the vicinity of 200°C. Singh & Ohring found that the effective charge number of Sn is dependent on temperature, and their reported values are a little bit smaller than those from Khosla & Huntington. Sorbello (Sorbello 1973) developed an electromigration theory, which is based on the pseudopotential calculation of driving forces for atomic migration in metals in the presence of electric current, and predicted effective charge number of Sn to be -10 at 185°C. Sorbello's theory favors the experimental results from Khosla & Huntington and Singh & Ohring. The effective charge number values vs. temperature from the aforementioned references are plotted in Figure 74.

The effective charge number of lead-free solder is chosen as $Z^* = -20$ at 30°C (measured stressing temperature) based on these references. This negative effective charge number is for the atoms in the solder, indicating that the atoms are actually migrating in the opposite direction of electric current. Since the vacancy migrates in the opposite direction of the moving atom, the effective charge number for the vacancy is positive. Therefore, in the simulation the effective charge number of vacancy is taken as $Z^* = 20$.

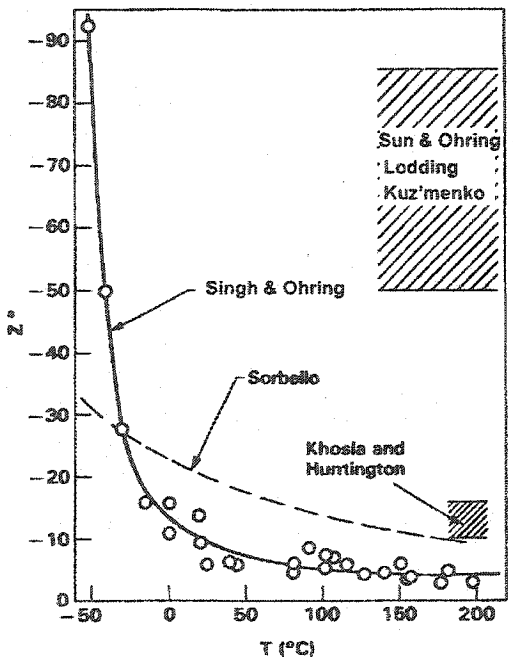


Figure 74 Effective charge number in Tin vs. Temperature (after Singh & Ohring (Singh and Ohring 1984))

D. Other Simulation Parameters for Lead-Free Solder Alloy

T=303K, temperature (assumed as uniformly distributed in the solder joint).

K=8.62×10^{-5}eV/K=1.38×10^{-23}J/K, Boltzman's constant.

τ_s=1.8×10^{-3}s, vacancy relaxation time (Sarychev and Zhinikov 1999).

f=0.6, average vacancy relaxation ratio (Sarychev and Zhinikov 1999).

ρ=1.15×10^{-5}$\Omega \cdot cm$, electrical resistivity.

E=41.4GPa=4.14×10^6N/cm^2, Young's modulus.

ν=0.33, Poisson's ratio.

4.3.3 FEM Simulation Model and Boundary Conditions

FlexPDE is used as the finite element code in the simulation. A brief description of this software can be found in Section 3.4 of Chapter 3. A 2-dimensional simulation model is employed in order to simplify the computational complexity. Figure 75 shows the simulation model and the displacement boundary conditions. This 2-D model is a simplification of the real test structure as shown in Figure 58. Both the horizontal and vertical displacements at the far ends of the bottom copper plate are assumed to be fixed due to the clamping of the fixture. The horizontal and vertical displacements at the far ends of the top copper plate are also assumed to be fixed due to the restriction from the embedded nylon spacer. The diffusion boundary condition assumes that vacancy fluxes on all the edges are zero (natural boundary condition).

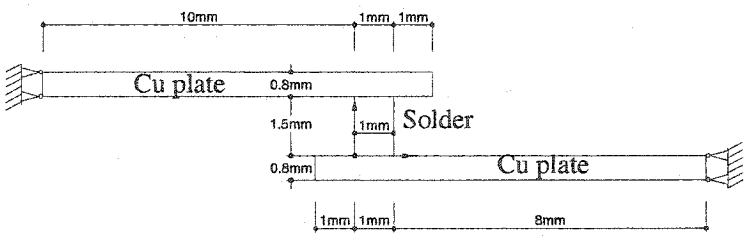


Figure 75 FEM model and Boundary conditions

Since the solder joint is polished to be a very thin film (0.2~0.3mm average in thickness), the plane stress assumption is applied to solder joint. On the other hand, the widths of the copper plates are over 40 times wider than the thickness of solder joint; therefore, the plane strain assumption is applied to copper plates. The plane strain formulation for the elastic mechanical stress-strain electromigration model is derived in

detail in Section 3.3 of Chapter 3. The plane stress formulation derivation is listed in the Appendix.

Assumptions for Copper Plates

Since the copper plates have a much larger cross-section than that of solder joint, electromigration is only expected in the solder joint. Therefore, the current density in the copper plate is assumed to be zero. To simplify the problem, the interface between the copper plate and solder joint is treated as a blocking boundary for solder diffusion by assuming that the diffusivity of copper is much smaller than that of solder. The volumetric strain at lattice site due to current stressing is explicitly treated as zero in the copper plate to further reduce the computational complexity. The material properties of copper are as follows:

E=117GPa=1.17×10^7N/cm^2, Young's modulus.

ν=0.33, Poisson's ratio.

4.3.4 Simulation Results of Module M-Pbfree-3

The first simulation case is module M-Pbfree-3 because most dramatic horizontal and vertical displacements were measured in this module. The simulations for other modules are presented in later sections. The width of the solder joint is 1mm and the height is 1.5mm. The thickness of the test solder joint is not uniform. The thinnest portion is a little less than 250μm and it is gradually thicker near the solder-copper plate interfaces as measured under a 100X optical microscope (Figure 76a).

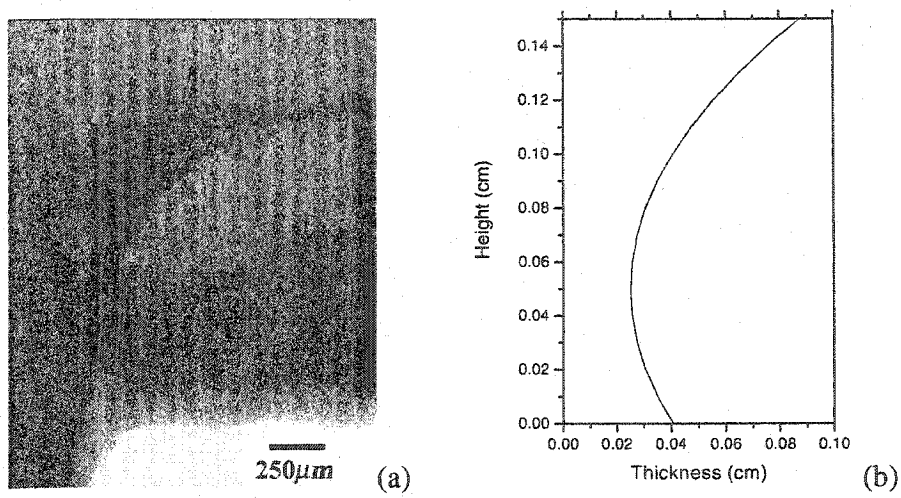


Figure 76 Thickness of solder joint of M-Pbfree-3 (a) Optical microscopic image (b) Thickness variation along the height of the solder joint used in the simulation

The non-uniform thickness leads to non-uniformity of the current density in the solder joint. This factor is taken into consideration in the simulation and it will be shown later that the non-uniformity of current density in the solder joint greatly affects the deformation evolution of solder joint under electric current stressing. In the simulation, the thickness of solder joint is assumed to be a continuous function of position along the height of the solder joint:

$$W_{thickness} = 0.025 \times [1 + 2.5 \times (\frac{y - 0.05}{0.1})^2] \qquad (4.11)$$

where $W_{thickness}$ is the thickness of solder joint, and y is the position along the height of the solder joint. The unit here is *cm*. The variation of thickness described by this function is shown in Figure 76(b). Since a two-dimensional simulation is employed, the variation of thickness cannot be directly introduced in the simulation model. Instead, it is considered by using a non-uniform stressing current density in the solder joint. The effect of the thickness variation on the mechanical behavior of the solder joint is not considered, where plane stress assumption is still taken. The current density in a 1*mm* wide and

0.25*mm* thick solder joint is $1.12\times10^4 A/cm^2$. The non-uniform current density along the height of the solder joint is therefore assumed in the simulation to be:

$$j = 1.12\times10^4 / [1 + 2.5\times(\frac{y - 0.05}{0.1})^2] \; (A/cm^2) \qquad (4.12)$$

where j is current density. The current density is assumed to be uniformly distributed along the width of the solder joint. The complete FlexPDE source code for this simulation is listed in the Appendix A-2.

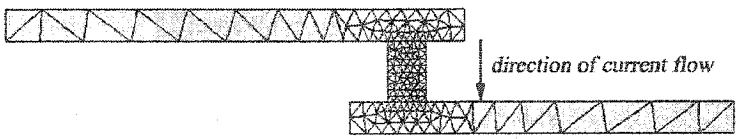
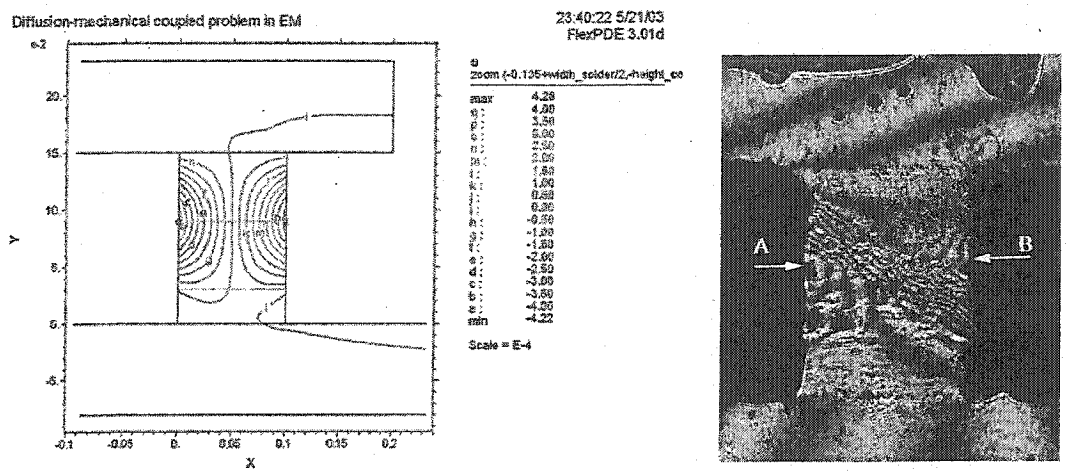


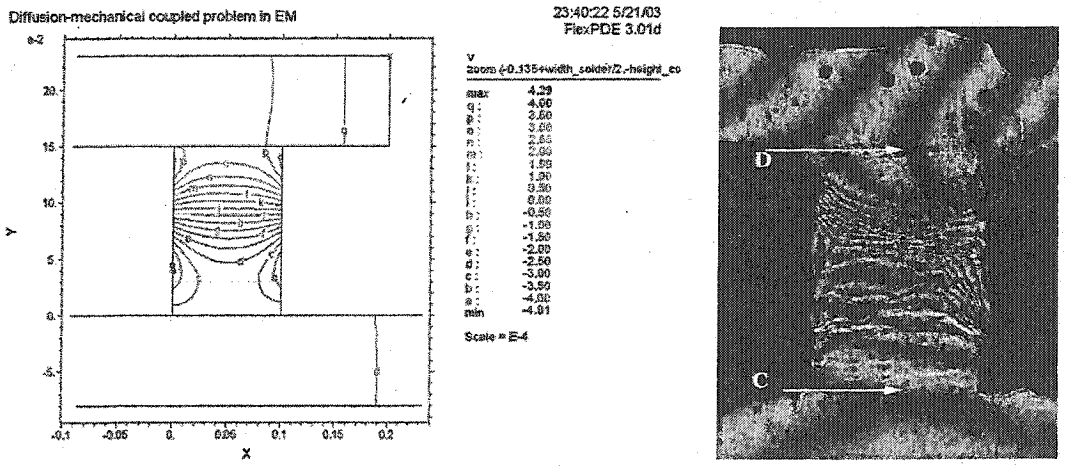
Figure 77 FEM simulation Mesh

Figure 77 shows the FEM simulation mesh. As mentioned before, the direction of current flow is from the upper copper plate to the lower copper plate. The current density in the copper plate is assumed to be zero since copper plate has much larger cross section than that of the solder joint. The following figures show length in *cm*, stress in N/cm^2, and time in *second*, unless otherwise noted.



(a) (b)

Figure 78 (a) Simulated horizontal displacement after 600 hours of current stressing (b) U field fringe development after 605 hours of current stressing



(a) (b)

Figure 79 (a) Simulated vertical displacement after 600 hours of current stressing (b) V field fringe development after 605 hours of current stressing

Figure 78 and Figure 79 show the simulated distributions of horizontal and vertical displacements within the solder joint along-side the Moiré Interferometry measurement after 600 hours of current stressing. They clearly show that the simulation results qualitatively match the measured displacement fields. The simulated distributions of both horizontal and vertical displacements resemble the distributions measured by the

experiment. Large normal deformation developed in the horizontal direction, but the horizontal normal deformations are not uniform along the both edges of the solder joint. Large transverse deformation also developed in the vertical direction. Figure 80 shows the distribution of transverse deformation along a vertical line between points C and D (Figure 79) after 600 hours of current stressing from both the simulation and experimental measurement. It is clear that they agree well. The transverse strain ε_y can be calculated from the experimental results by numerically differentiate the relative transverse displacement with respect to vertical coordinate, or $\varepsilon_y = dV/dy$.

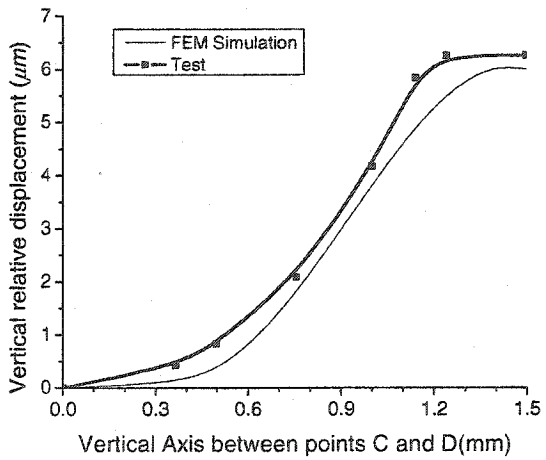


Figure 80 Vertical relative displacement V distribution from point C to D after 600 hours of current stressing from FEM simulation and experimental measurement

Figure 81 compares the results of transverse strain ε_y distribution along a vertical line between points C and D (Figure 79) after 600 hours of current stressing from both the FEM simulation and the experimental measurement. It shows that the transverse strains ε_y calculated from the FEM simulation and the experimental measurement are on the same order of magnitude and have the similar distribution. Figure 82 compares the results of normal strain ε_x distribution along a horizontal line between points A and B (Figure 78) after 600 hours of current stressing. They are also on the same order of

magnitude. However, the normal strains calculated from the experimental measurement are generally smaller than those from the FEM simulation. Figure 83 compares the results of shear strain τ_{xy} distribution along a vertical line between points C and D (Figure 79) after 600 hours of current stressing. Quite different from the comparisons of normal and transverse strain, the shear strains are very different between the FEM simulation and those calculated from experimental results. The FEM simulation predicts very small shear strain along the vertical line between points C and D; however, the shear strains calculated from the the experimental results are quite large. We think that the measured shear strains are due to the thermal deformation in the experiment. As mentioned in the previous section, despite better thermal management, there was still some temperature increase during current stressing. On the other hand, no thermal deformation was considered in the FEM simulation. In order word, the thermal deformations in the experiment contribute to this decrepency.

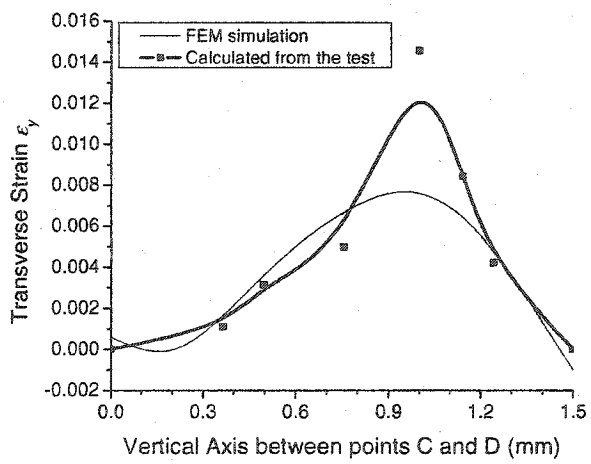


Figure 81 Vertical transverse strain ε_y distribution from point C to D after 600 hours of current stressing from FEM simulation and experimental measurement

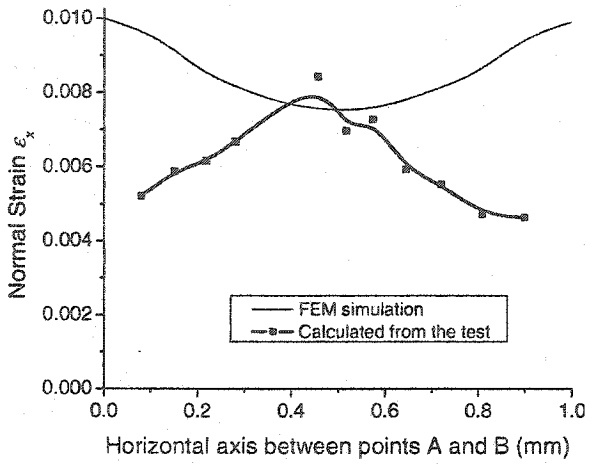


Figure 82 Horizontal normal strain ε_y distribution from point A to B after 600 hours of current stressing from FEM simulation and experimental measurement

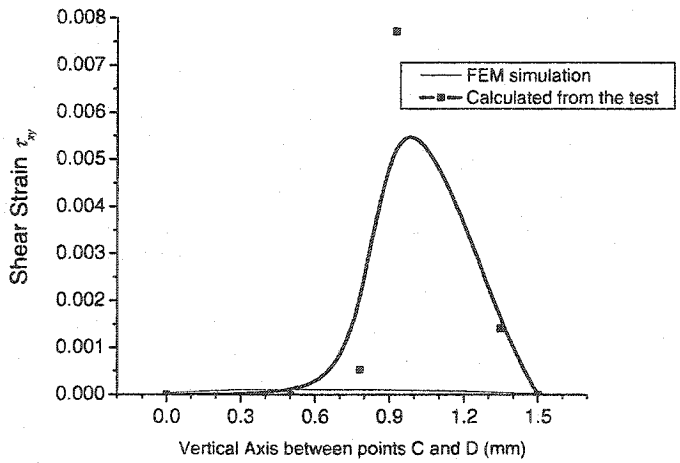


Figure 83 Shear strain τ_{xy} distribution from point C to D after 600 hours of current stressing from FEM simulation and experimental measurement

The simulation results are not exactly the same as the experimental measurements, but considering all the assumptions (solder diffusivity, effective charge number, thermal equilibrium vacancy concentration, vacancy relaxation time, etc.) that were taken and the many simplifications (the thickness variation of the solder joint, 2-D simplification of the 3-D structure, the treatments of copper plates and solder-copper interface, elastic assumption of the mechanical constitutive model for lead-free solder alloy, etc.) of the simulation model, the simulation results are quite reasonable.

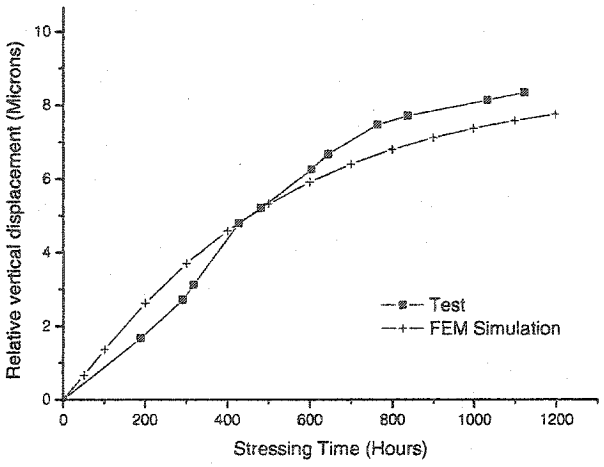


Figure 84 Evolution of relative vertical displacement between lower and upper interface of solder joint (points C and D) and copper plates in M-Pbfree-3

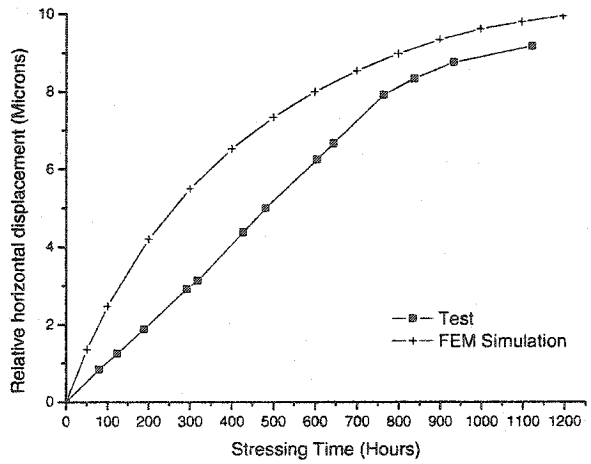


Figure 85 Evolution of maximum relative horizontal displacement between the two edges of the solder joint (points A and B) in M-Pbfree-3

As shown in Section 4.2.2, the fringes measured in the solder joint gradually increase with stressing time and reached steady state after 1000 hours of stressing. The simulation results show a similar trend. The maximum relative vertical displacement between the solder-copper interfaces (relative vertical displacement between points C and D in Figure 79(b)) and maximum relative horizontal displacement between the two edges of the solder joint (relative horizontal displacement between points A and B in Figure 78(b)) are chosen to compare their time history evolutions between the simulation results and experimental measurements. Figure 84 shows the comparison of maximum relative

vertical displacement between the two copper-solder interfaces. The FEM simulation predicts higher than experimental measured values for the first 500 hundred hours of current stressing and lower values after 500 hours of stressing. The simulation indicates the increase rate of relative vertical displacement decrease with stressing time; whereas, the experimental observation shows the largest increase rate of relative vertical displacement took place between 300 to 800 hours of current stressing. Both simulation and experimental results show that the relative vertical displacement approached steady state after 1000 hours of current stressing. Figure 85 shows the evolution of maximum relative horizontal displacement between the two edges of the solder joint. The FEM simulation result is always higher than the experimental result and they both approach steady state after 1000 hours of current stressing. As shown in these two figures, the simulated time history evolution results closely match the experimental results, although they are not identical. Therefore, both the spatial distribution and time history evolution of the displacements confirm that the electromigration model used in this simulation is valid for lead-free solder alloy.

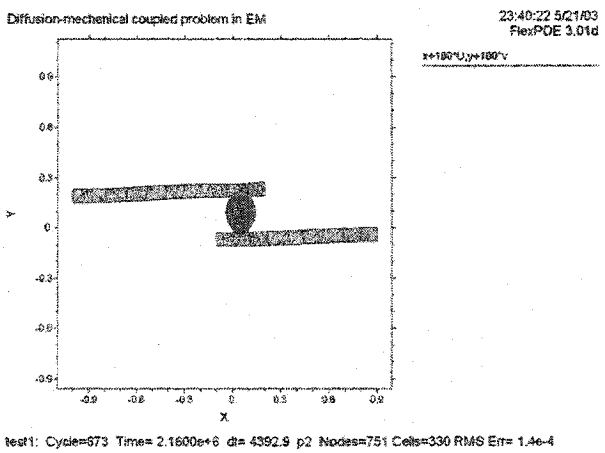


Figure 86 Simulated deformation of M-Pbfree-3 after 600 hours of current stressing

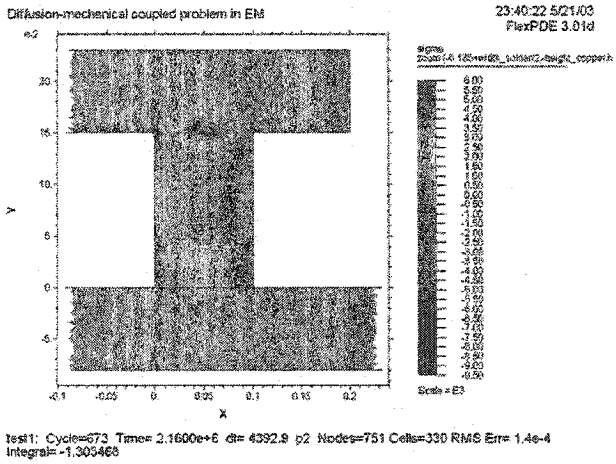


Figure 87 Simulated spherical stress distribution in M-Pb-free-3 after 600 hours of current stressing

Figure 86 shows the exaggerated deformed shape of the test module after 600 hours of current stressing. The simulated spherical stress distribution within M-Pbfree-3 after 600 hours of current stressing is shown in Figure 87. Both the maximum positive and negative spherical stresses occur on the interface between the upper copper plate and the solder joint. The maximum spherical stress is on the order of $60MPa$. Figure 88 to Figure 90 show the distributions of normal, transverse, and shear strains ε_x, ε_y, and γ_{xy} within M-Pbfree-3 after 600 hours of current stressing. The normal and transverse strains are found to be dominant and on the order of 1%. The shear strain is found highly localized within the solder joint and its maximum value is only on the order of 0.4%, which is much smaller than the maximum normal strains. The strains are found to be almost symmetric along the vertical center line, but these strains are non-symmetric along the horizontal center line. This is due to the non-uniform distribution of current density within the solder joint, as assumed in Equation (4.12). The distributions of normal, transverse, and shear stresses, σ_x, σ_y, and τ_{xy}, within M-Pbfree-3 after 600 hours of current stressing are shown in Figures 91-93. The maximum positive and negative normal

stress, σ_x, is found to be on the interface of upper copper plate and solder joint and is on the order of $120MPa$. The maximum normal stress, σ_y, is found to be on the both edges of the solder joint and is on the order of $120MPa$. Like the shear strain, the shear stress is localized within the solder joint and its maximum value is on the order of $60MPa$. The symmetries of the stresses are similar to that of strains due to distribution of current density.

In the simulation, the author used elastic constitutive model for solder alloy. Almost all other researches on electromigration used elastic assumption. However, as shown in our simulation, the stresses in the solder joint are much higher than the yield stress of solder (around 30MPa). The solder alloy is a viscoplastic material which creeps even at room temperature. This result demonstrates the need to use viscoplastic constitutive mdoel for solder alloy in electromigration analysis.

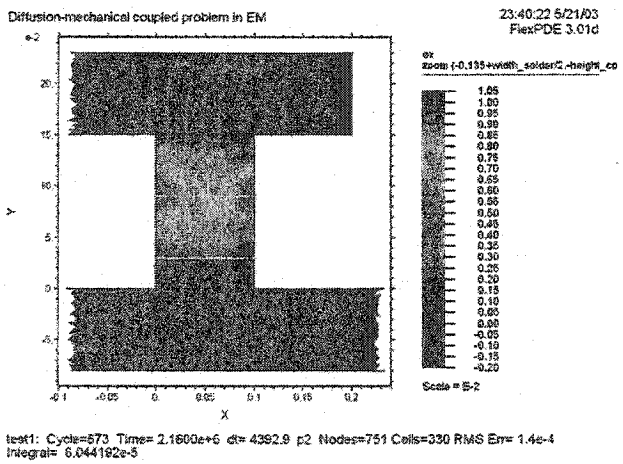


Figure 88 Simulated normal strain ε_x distribution after 600 hours of current stressing

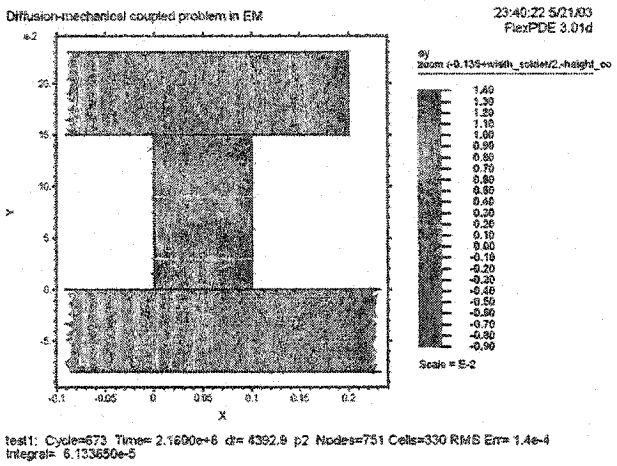


Figure 89 Simulated transverse strain ε_y distribution after 600 hours of current stressing

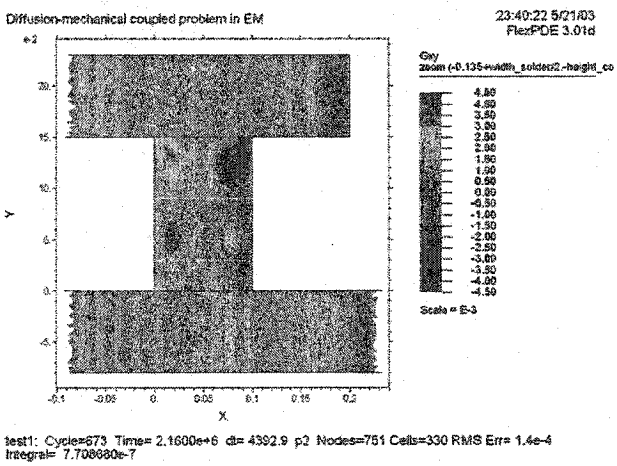


Figure 90 Simulated shear strain γ_{xy} distribution after 600 hours of current stressing

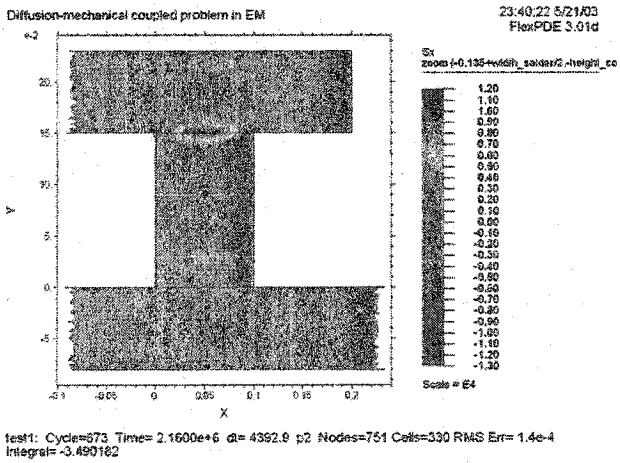


Figure 91 Simulated normal stress σ_x distribution after 600 hours of current stressing

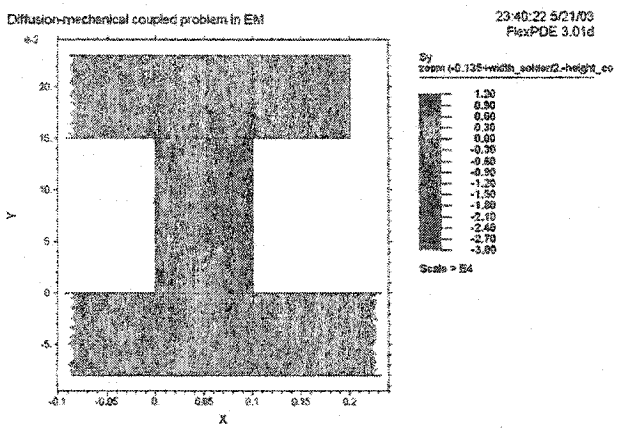


Figure 92 Simulated normal stress σ_y distribution after 600 hours of current stressing

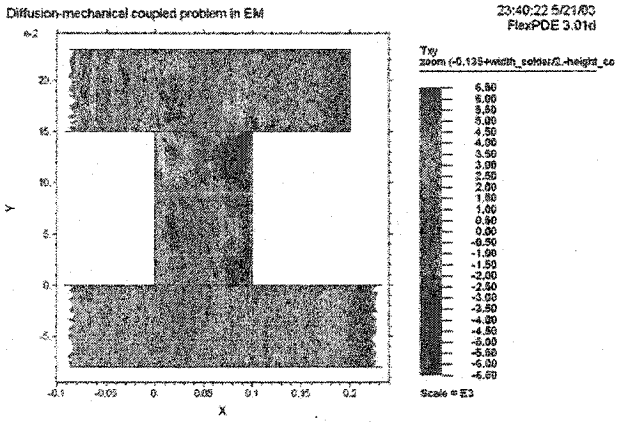


Figure 93 Simulated shear stress τ_{xy} distribution after 600 hours of current stressing

In this section, the deformation simulation of M-Pbfree-3 under high current density stressing is conducted by employing the electromigration model described in Section 4.3.1. The solder joint is modeled with the plane stress assumption; while the copper plates are modeled with the plane strain assumption in order to account for the great difference in thickness in a two-dimensional simulation. It is assumed that electromigration is only taking place in the solder joint since the current densities in copper plates are very low. The interfaces between the copper plates and the solder joint are simplified as blocking boundaries. The variation in thickness of the solder joint is

considered by applying a non-uniform current density within the solder joint. The mechanical constitutive model of both solder alloy and copper are assumed to elastic. Despite all of the assumptions and simplifications employed in the simulation, the displacements results are reasonably close to the Moiré Interferometry experimental results in both spatial distribution and time history evolution. This indicates that the electromigration model employed in this simulation is reasonably good at predicting the deformation behavior of lead-free solder alloy under electric current stressing.

The FEM simulation predicts that during current stressing both the horizontal and vertical displacement fields will be symmetric with respect to the central vertical line of solder joint, as shown in Figure 78(a) and Figure 79(a). Figure 78(b) and Figure 79(b) show that the Moiré interferometry fringes in the U and V fields are not perfectly symmetrical to the central vertical line.

The author believes that this discrepancy comes from the thickness assumption in the solder joint. In the simulation, the variation of the thickness of the solder joint along its height is considered, but the thickness along the width of solder joint at any height is assumed to be the same. This may not be the case. The non-uniformity of the thickness of the test solder joint along its width contributes to the non-symmetric observation of its Moiré interferometry fringes. Thermal expansion can also contribute to the non-symmetric observation of Moiré interferometry fringes, which is not considered in the simulation.

Another discrepancy between the simulation results and the experimental observation is the displacements time history evolution. As shown in Figure 84, the simulation result of relative vertical displacement between the lower and upper interfaces

of the solder joint and the copper plates is higher than the experimental observation during the first 500 hours of current stressing and is lower after that. The simulation result of maximum relative horizontal displacement between the two edges of the solder joint is always higher than experimental observation as shown in Figure 85. This discrepancy comes from the many assumptions that are used in the simulation. All the diffusion and electromigration parameters of lead-free solder alloy, such as atomic diffusivity, vacancy diffusivity, thermal equilibrium vacancy concentration, and effective charge number, used in the simulation are taken from the diffusion and electromigration experiments of pure tin because there are few experiments in this area done for lead-free solder alloy. The simulation results should improve when more diffusion and electromigration data are available for lead-free solder alloys.

4.3.5 Simulation Results of Modules M-Pbfree-4 and M-Pbfree-1

As shown in Section 4.2.2, the average stressing current density in the solder joint of M-Pbfree-4 is $1.33\times10^{4} A/cm^{2}$, which is higher than that in M-Pbfree-3 ($1.12\times10^{4} A/cm^{2}$). But contrary to our expectation, the Moiré interferometry fringes in both U and V fields are far fewer than those observed in M-Pbfree-3. This result shows that the current density is not the only factor dominating the fringe or displacement development in the solder joint during current stressing. In the following simulations, the current density distribution is found to be another important factor that affects the displacement development in the solder joint during current stressing.

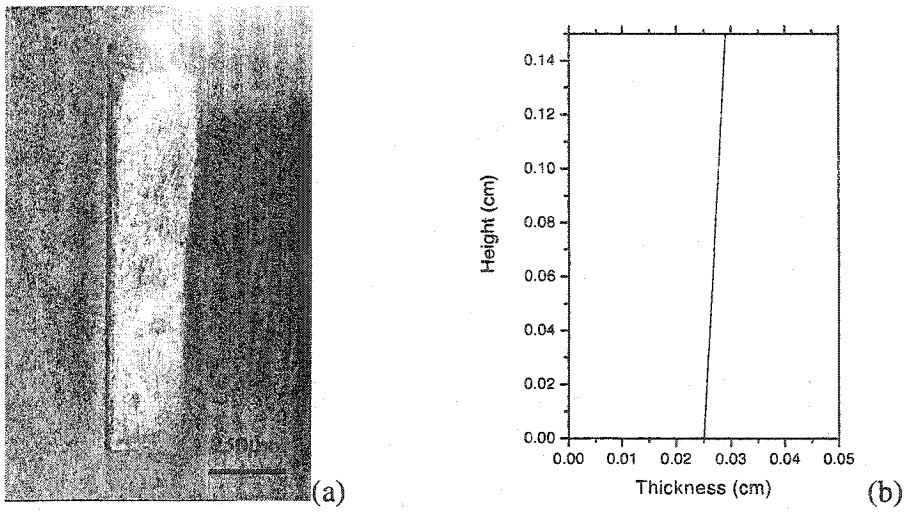


Figure 94 Thickness of solder joint of M-Pbfree-4 (a) Optical microscopic image (b) Thickness variation along the height of the solder joint used in the simulation

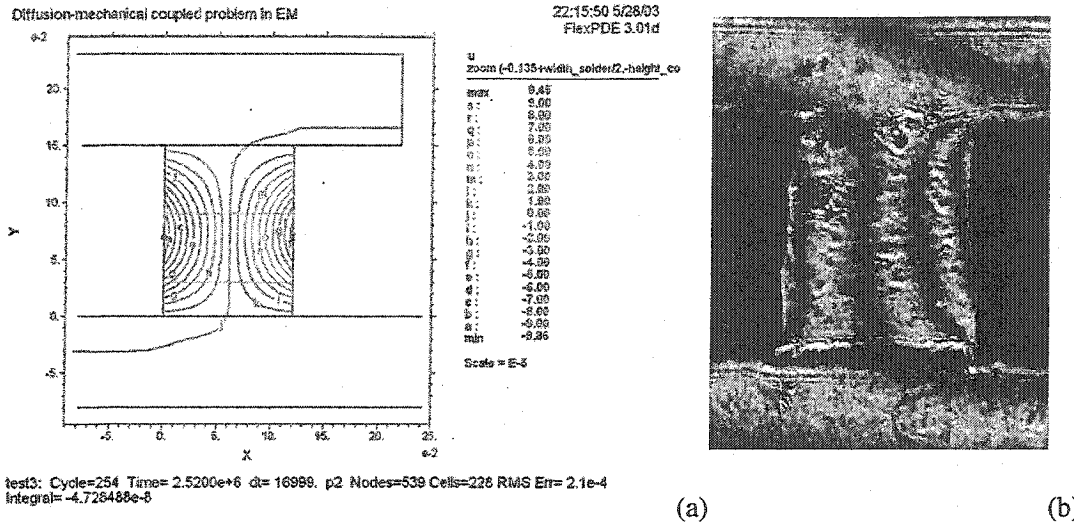
The width of the solder joint in M-Pbfree-4 is 1.2*mm* and the height is 1.5*mm*. The average thickness of the solder joint is 0.25*mm* and it is a little bit thicker near the interface between the upper copper plate and solder joint. As in the simulation of M-Pbfree-3, the variation of thickness is taken into account in the simulation. The thickness of solder joint is assumed to be described by the following function (Figure 94):

$$W_{thickness} = 0.025 \times (1 + 0.15y / 0.15) \tag{4.13}$$

where $W_{thickness}$ is the thickness of solder joint, and y is the position along the height of the solder joint. The unit here is *cm*. This variation is implemented in the simulation by applying a non-uniform stressing current density:

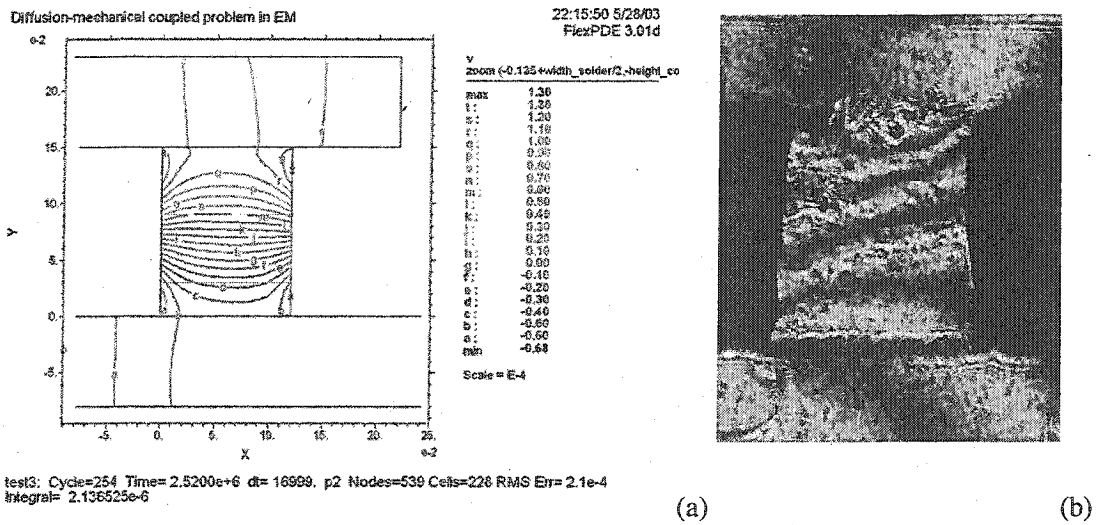
$$j = 1.33 \times 10^4 / (1 + 0.15y / 0.15)\,(A / cm^2) \tag{4.14}$$

where j is current density.



(a) (b)

Figure 95 (a) Simulated horizontal displacement after 700 hrs of current stressing in M-Pbfree-4 (b) U filed fringe development after 690 hours of current stressing



(a) (b)

Figure 96 (a) Simulated vertical displacement after 700 hrs of current stressing in M-Pbfree-4 (b) V filed fringe development after 690 hours of current stressing

Figure 95 and Figure 96 show the simulated distributions of horizontal and vertical displacement within the solder joint after 700 hours of current stressing along the side with the Moiré Interferometry measurement. The simulation results of both horizontal and vertical displacements resemble the measured displacement distributions from the experiments. The value of maximum relative horizontal displacement between

the two edges of the solder joint predicted by the FEM simulation is 1.928μm while the experiment found it to be 1.46μm. The value of relative vertical displacement between the upper and lower copper-solder interfaces predicted by the simulation is 1.476μm while the experimental observation is 1.668μm. The results from simulation are close to the experimental observations. The calculation of strains from the experimentally measured displacements is not performed for module M-Pbfree-4 and M-Pbfree-1 because reasonable accuracy of extracted strains cannot be achieved for these modules. The strains are extracted by numerically differentiate the measured displacements as described in Section 4.1. This numerical differentiation process generally gives good accuracy of extracted strain from fringe measurement when the data points for interpolation are sufficient. When very few data points (indicating small variation of displacements in x or y direction, but not necessary small strains) are available (which is the case for M-Pbfree-4 and M-Pbfree-1) for interpolation, a loss of accuracy of an order of magnitude in numerical differentiation is possible (Post et al. 1994).

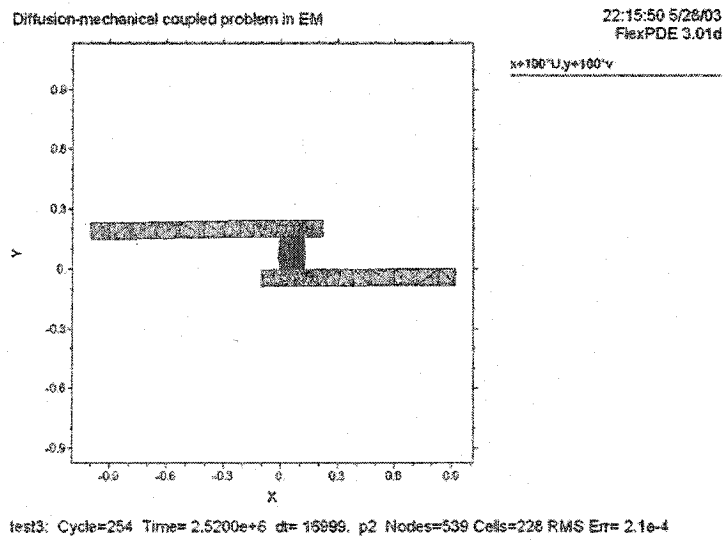


Figure 97 Simulated deformation of M-Pbfreee-4 after 700 hours of current stressing

The exaggerated deformation of the test module after 700 hours of current stressing from the simulation is shown in Figure 97. The comparison of time history evolution of the relative vertical displacement between the upper and lower copper-solder interfaces is shown in Figure 98. Figure 99 shows the comparison of time history evolution of the maximum relative horizontal displacement between the two edges of the solder joint. Both the simulation results and experimental observations show that the developments of these displacements approach steady state after 900 hours of current stressing. The time history evolution curves from the experimental observation look rough. This is because the displacement resolution of the Moiré Interferometry technique, which is defined by the frequency of diffraction grating (1200 *lines/mm*), is 0.417μm per fringe order in our experiment. Changes in displacement cannot be measured accurately if they are less than 0.417μm. As shown in these two figures, the simulation results are close to the experimental observations.

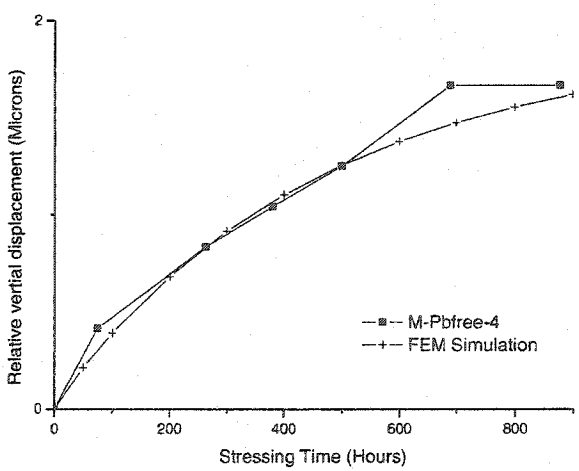


Figure 98 Evolution of relative vertical displacement between lower and upper interface of solder joint and copper plates in M-Pbfree-4

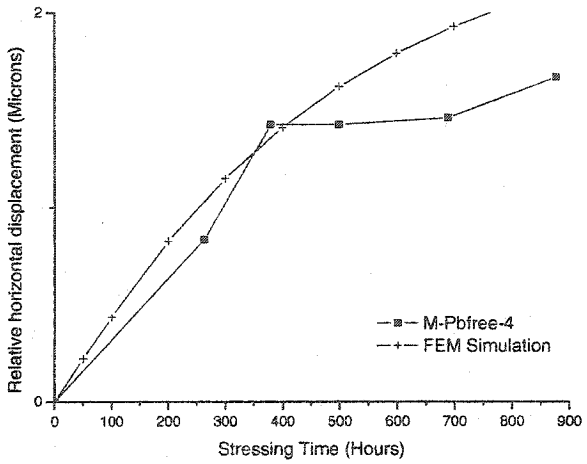


Figure 99 Evolution of maximum relative horizontal displacement between two edges of the solder joint and copper plates in M-Pbfree-4

As mentioned in the beginning of this section, the observed Moiré interferometry fringes in both the U and V fields of M-Pbfree-4 are far fewer than those of M-Pbfree-3 even though the current density in M-Pbfree-4 is higher than that in M-Pbfree-3. The biggest difference between these two modules is the thickness variation in the solder joint. M-Pbfree-3 has much more dramatic thickness variation than M-Pbfree-4. In the simulations, the thickness variation is taken into consideration by the means of non-uniform current density within the solder joint. The current density variation within the solder joint in the simulation of M-Pbfree-3 is much larger than that in the simulation of M-Pbfree-4. The simulation results show that larger current density variation leads to larger displacements in the solder joint. For example, after 700 hours of current stressing, the simulations predict the maximum relative horizontal displacement between the two edges of solder joint to be 8.45μm for M-Pbfree-3 comparing to 1.928 μm for M-Pbfree-4 despite the maximum current density used in the simulation of M-Pbfree-4 is higher than that used in the simulation of M-Pbfree-3. The simulation prediction of relative vertical displacement between the upper and lower copper-solder interfaces after 700 hours of

current stressing for M-Pbfree-3 is 6.4μm while it is 1.476μm for M-Pbfree-4. Therefore, both the experimental observations and FEM simulation indicate that current density distribution within the solder joint has a great effect on the displacement development in the solder joint under current stressing. More specifically, larger current density non-uniformity leads to larger normal deformations within the solder joint in this test module.

The width of the solder joint in M-Pbfree-1 is 1.35mm and the height is 1.5mm. The average thickness of the solder joint is 0.25mm and is a little bit thicker near the both interfaces between the copper plates and solder joint. As in the previous simulations, the variation of thickness is taken into account in the simulation. The maximum current density in the solder joint is 6000A/cm^2.

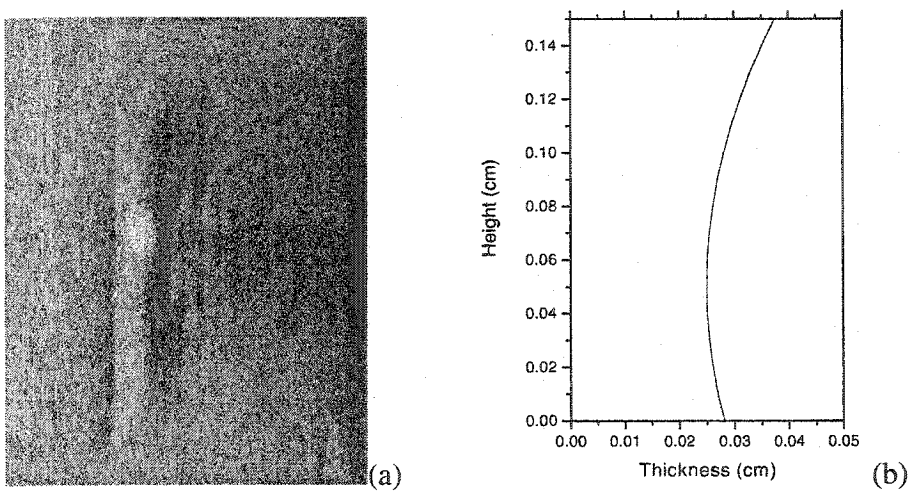


Figure 100 Thickness of solder joint of M-Pbfree-1 (a) Optical microscopic image (b) Thickness variation along the height of the solder joint used in the simulation

The thickness of solder joint is assumed to be described by the following function (Figure 100):

$$W_{thickness} = 0.025 \times (1 + 0.5 \times (\frac{y - 0.1}{0.1})^2) \tag{4.15}$$

where $W_{thickness}$ is the thickness of solder joint, y is the position along the height of the solder joint. The unit here is cm. This variation is implemented in the simulation by applying a non-uniform stressing current density:

$$j = 0.6\times10^4 /(1+0.5\times(\frac{y-0.1}{0.1})^2)\,(A/cm^2) \qquad (4.16)$$

where j is current density.

Figure 101 and Figure 102 show the simulated distributions of horizontal and vertical displacement within the solder joint along the side with the Moiré interferometry measurement after 200 hours of current stressing. The simulation results of both horizontal and vertical displacements resemble the measured displacement distributions from the experiments. The value of maximum relative horizontal displacement between the two edges of the solder joint predicted by FEM simulation is $0.62\mu m$ and is in expansion, while the experiment found it to be $0.834\mu m$. The value of relative vertical displacement between the upper and lower copper-solder interfaces predicted by the simulation is $0.898\mu m$ and is also in expansion, while the experimental observation is $0.834\mu m$. The results of simulation are close to the experimental observations.

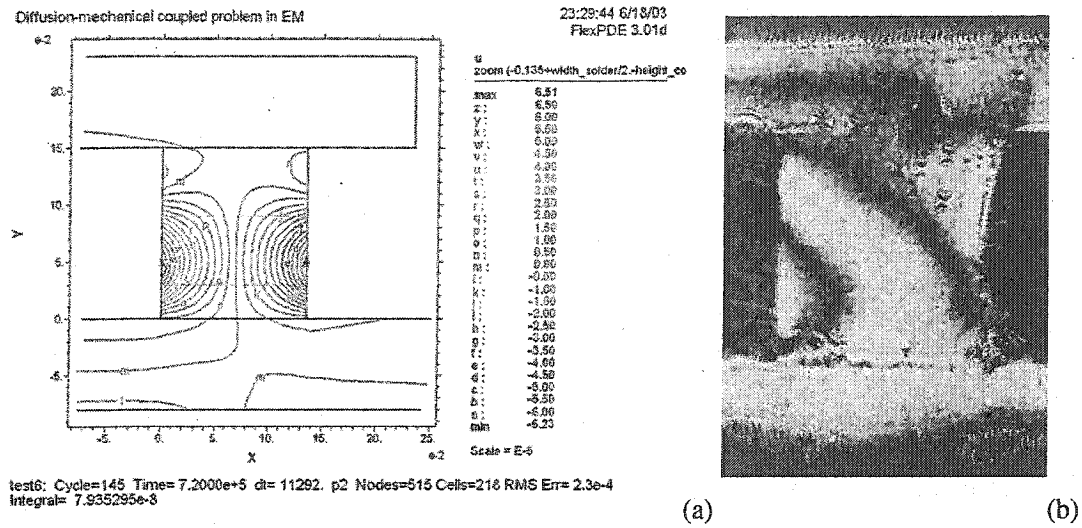


Figure 101 (a) Simulated horizontal displacement after 200 hrs of current stressing in M-Pbfree-1 (b) U filed fringe development after 239 hours of current stressing

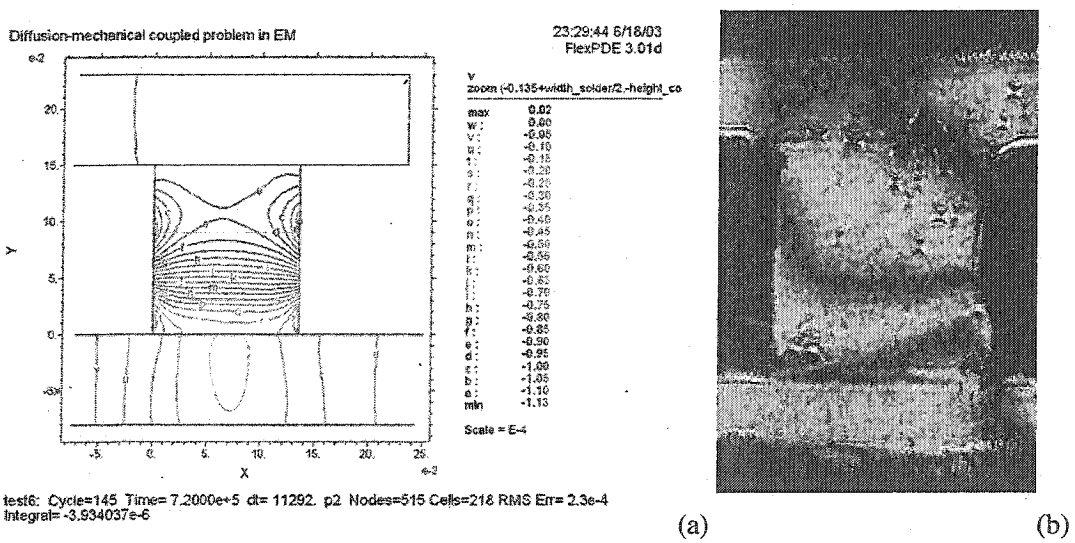


Figure 102 (a) Simulated vertical displacement after 200 hrs of current stressing in M-Pbfree-1 (b) V filed fringe development after 239 hours of current stressing

4.3.6 Simulation Results of Module with Ideally Uniform Thickness

In the previous simulations, the thicknesses of the solder joints are assumed to be non-uniform due to the non-uniform thickness of the test module. In this section, a numerical simulation of a test module with uniform solder thickness is reported. The

results show that if the thickness of solder joint is ideally uniform, the deformation within the solder joint is much smaller than that in a solder joint with non-uniform thickness. In the simulation, the width of the solder joint is assumed to be $1mm$ and the height to be $1.5mm$. The current density within the solder joint is assumed to be uniformly distributed as $1.2\times10^{4}A/cm^{2}$. Figure 103 and Figure 104 show the simulated horizontal and vertical displacements fields after 1000 hours of current stressing. The maximum displacement within the solder joint under uniform current density stressing is on the order of 10^{-4} μm, which is orders of magnitude smaller than that for the non-uniform current density case (on the order of μm) under the same magnitude of current density stressing ($10^{4}A/cm^{2}$).

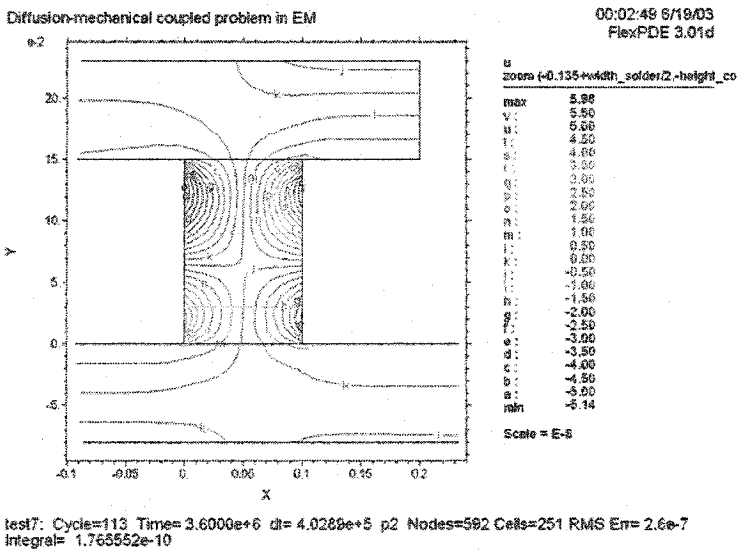


Figure 103 Simulated horizontal displacement field after 1000 hours of current stressing for uniformly distributed current density

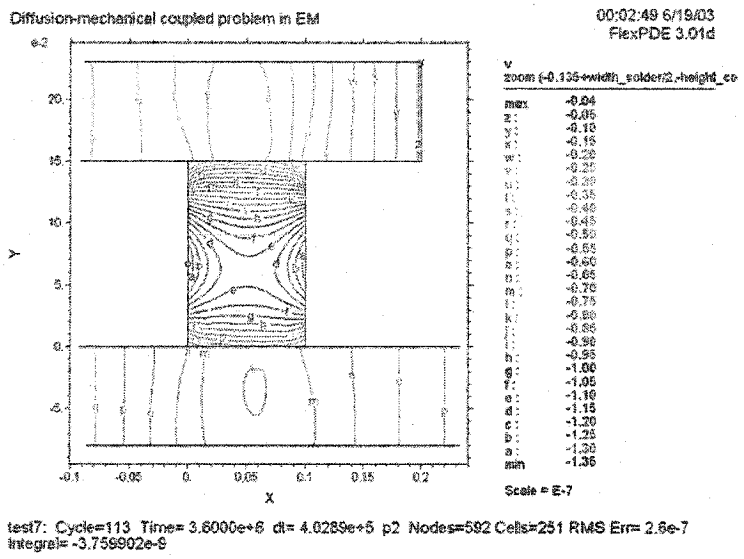


Figure 104 Simulated vertical displacement field after 1000 hours of current stressing for uniformly distributed current density

Figures 105-107 show the simulated stress distributions within the solder joint after 1000 hours of current stressing. It is clear that the stress build-up within the solder joint under uniform current density stressing is very small (on the order of $10^{-2}\,MPa$) compared to the cases of non-uniform current density stressing (on the order of $100MPa$).

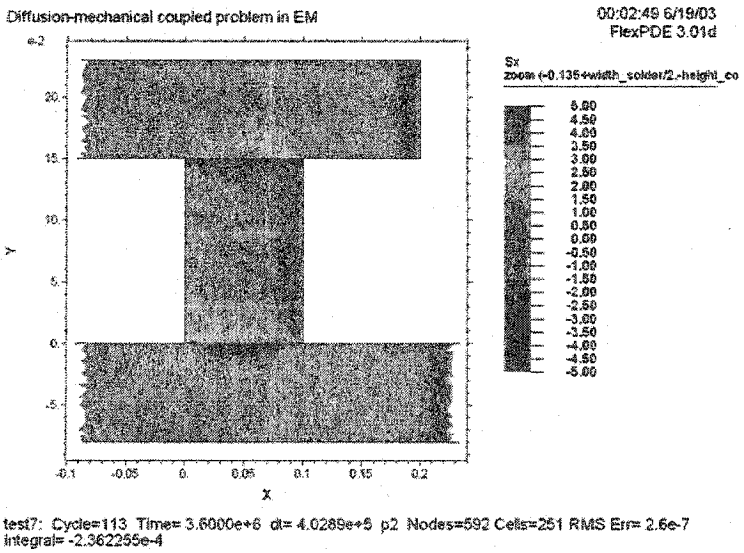


Figure 105 Simulated normal stress σ_x distribution after 1000 hours of current stressing for uniformly distributed current density

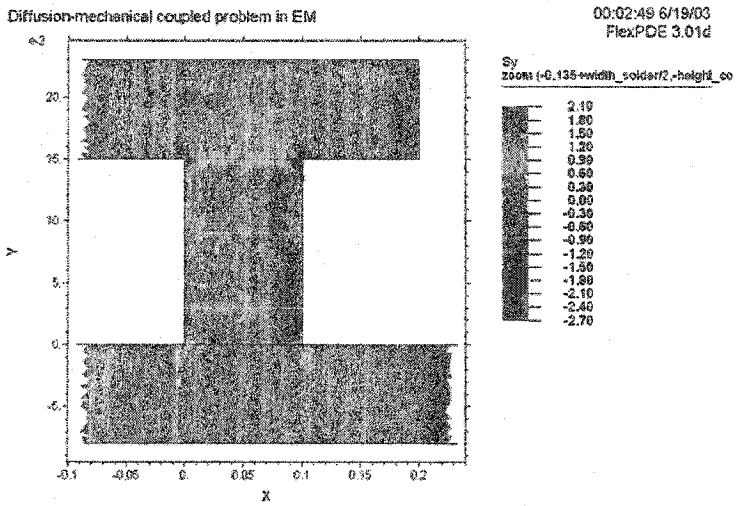


Figure 106 Simulated normal stress σ_y distribution after 1000 hours of current stressing for uniformly distributed current density

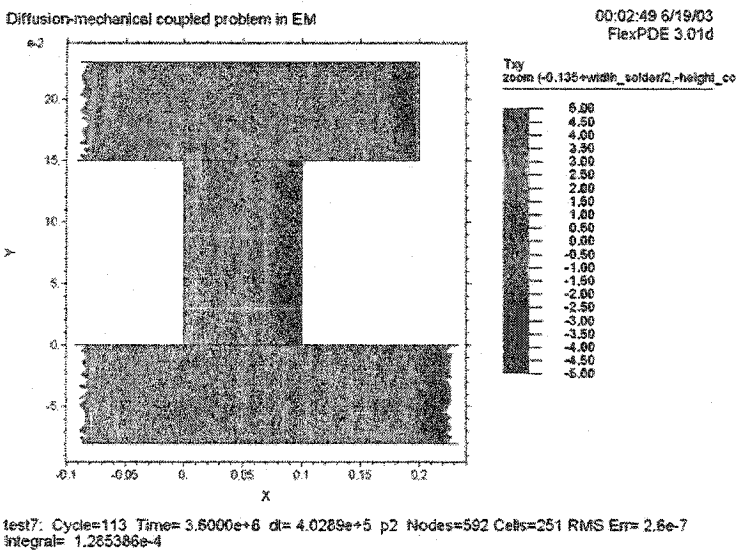


Figure 107 Simulated shear stress τ_{xy} distribution after 1000 hours of current stressing for uniformly distributed current density

4.4 Discussions

In this chapter, the Moiré Interferometry technique is used to measure the in-situ displacement evolution of BGA solder joint under electric current stressing. First, the technique is verified by a low current density stressing experiment. Later, the improved

Moiré Interferometry experiments with thermal control distinguish deformations of the solder joints due to pure current stressing above 5000 A/cm^2. It is observed that high current density creates large deformation in the BGA solder joints. The experiments also suggest that this development takes several hundreds of hours since it is controlled by a diffusion-mechanical coupled process. These deformations are largely normal and transverse deformations, and the shear deformation is small. After the current is turned off, the deformations in the solder joints remain unchanged. This indicates that the deformations created by high current density are irreversible. However, these irreversible deformations are not the same as the plastic deformation. Plastic deformations are created by the high deviatoric (shear) stresses and correspond to the motion of large numbers of dislocations. The deformation created by electromigration is due to the re-arrangement of vacancies and atoms in the material as well as vacancy generations and annihilation due to diffusion and correspond to the volumetric strain at lattice site. However, as demonstrated in the numerical simulations, volumetric deformations at lattice site due to electromigration give rise to high level stresses that exceed the yield stress of the solder alloy, these high deviatoric stresses may create plastic deformations. Therefore, the irreversible deformations we observed in the experiments are the combination of electromigration deformations and plastic deformations.

The electromigration constitutive model presented in Chapter 3 is applied to simulate the deformation evolution of lead-free solder joint under current stressing. Despite all of the assumptions and simplifications employed in the simulation, it predicts reasonably close displacement results to the Moiré Interferometry experimental results in both spatial distribution and time history evolution. This indicates that the

electromigration model employed in this simulation is reasonably good at predicting the mechanical behavior of lead-free solder alloy under electric current stressing. The simulation results show that the high stresses that exceed the yield stress of the solder alloy can be developed in the solder joints. This indicates that elastic assumption, which is employed by most of the researchers on electromigration, is not sufficient to model the deformation and stress evolution in solder joints under high current density. Since solder alloy is viscoplastic even at room temperature, viscoplastic model is need to model the electromigration in solder joints. However, since the electromigration model proposed in this study does not need elastic assumption, viscoplastic constitutive model for solder alloy can be added easily.

Both the experimental observations and FEM simulation indicate that, in addition to the current density level, the current density distribution within the solder joint has a significant effect on the displacement development in the solder joint under current stressing. More specifically, larger current density non-uniformity leads to larger deformations in the solder joint in our module. This suggests that current crowding effect is important in electromigration, since it creates significant current density non-uniformity.

Chapter 5

Microstructural Evolution and Failure Modes of Flip-Chip Solder Joint under current stressing

5.1 Introduction

This chapter studies the reliability of flip-chip solder joints under high density electric current stressing. More than 20 flip-chip test modules were tested with different current densities and stressing temperatures. During current stressing, heat is also generated due to joule heating. In a typical flip-chip module, the cross-section area of the metal trace on the silicon dies is much smaller than that of the solder joint. Thus the primary heat source is the metal trace, which contributes to the most of the electric resistance of the module. The joule heating during current stressing may maintain a thermal gradient in the solder joint. Thermal migration is reported in Pb-In solder alloy at a thermal gradient of $1200^{o}C/cm$ by Roush et al (Roush and Jaspal 1982). Therefore, thermomigration is also a reliability concern for flip-chip solder joints. The experiments show that there is significant thermomigration due to the thermal gradient within the solder joint caused by joule heating during current stressing. A three dimensional coupled thermal electrical finite element analysis (FEA) shows the existence of a thermal gradient in flip-chip solder joint during current stressing. The failure of the module is caused by the combined effects of electromigration and thermomigration.

The failure modes of flip-chip solder joints under current stressing are analyzed based on the experiments of 20 flip-chip modules. Three different failure modes were

reported. The failure Mode caused by the combined effect of electromigration and thermomigration is characterized as that void nucleation and growth contributes the ultimate failure of the module. The void nucleation and growth in solder joint during current stressing is discussed in detail. The Ni UBM-solder interface is found to be the favorite site of void nucleation and growth. The effect of pre-existing voids on the failure process of solder joint is found to be dependent on their location. The time to failure of the test modules is found to generally obey Black's law (Black 1967) but with certain exceptions. The exceptions are due to different failure mechanisms in these test modules.

The microstructural evolution of the solder joint was monitored using Scanning Electron Microscopy (SEM) and, in some cases, it was quantified with the digital image processing technique. Pb Phase coarsening was observed under different current densities and temperatures. Higher current density leads to faster grain coarsening. Based on the test results, a grain coarsening equation that includes the influence of current density is proposed. The degradation of mechanical properties of solder joint during current stressing was tested with instrumented indentation testing (IIT) technique. The nano-indentation tests suggest that mechanical properties, such as the Young's modulus, degrade in the localized area where voids nucleate during current stressing.

5.2 Experimental Set-up and Preliminary Test

A preliminary test was first conducted to gain experience to improve the experimental procedure for later experiments. Three flip-chip modules were used in this preliminary experiment. Only Module #1 was subjected to current stressing at ambient atmosphere. The temperature of the solder joint during current stressing was not

measured in this test. Modules #2 and #3 were used in nano-indentation tests and provided initial mechanical properties of the solder joint prior to current stressing. Only solder joint A on each module was subjected to SEM analysis and the nano-indentation test. Mass accumulation near the anode and void nucleation near the cathode were observed during current stressing. Surface marker movement is used to measure the atomic flux driven by electromigration, and to calculate the product of effective charge number and diffusivity, DxZ^*, of the solder at room temperature.

5.2.1 Experimental Set-up

The test flip-chip modules were produced in an industrial lab at Motorola to attain consistent interconnects representative of volume manufacturing. The test module has a dummy silicon die with only an Aluminum (Al) conductor trace on it. The silicon die is attached to an FR4 printed circuit board (PCB) through eutectic Pb/Sn solder joints. The copper plates on the PCB provide the wetting surface and electric connection to the solder joints. The under bump metallization (UBM) on silicon die side is electroless nickel (Ni). The solder joints are encapsulated in the underfill between the silicon die and PCB. The thickness of the Al trace is about 1 μm and the width is about 150 μm. The diameter of the solder joint is around 150 μm and the height is about 100 μm. The test module was cross-sectioned and finely polished to the center of the solder joints before current stressing which reduced the thickness of the solder joint. Two solder joints were tested on each module. The solder joints on each test module are named in such a way that current always flows from copper trace through solder joint A into the Al trace on silicon die and then through solder joint B out to another copper trace. Figure 108 shows

a schematic cross-section of the test module and the direction of current flow in the experiments. Figure 109 shows the SEM secondary image of solder joint A on Module #3. During the course of current stressing, the test modules were taken off the circuit for scanning electron microscopy (SEM) inspection.

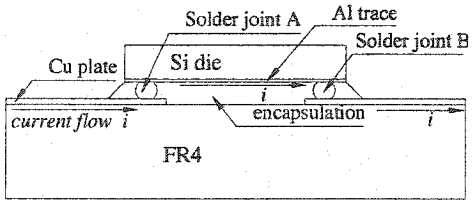


Figure 108 Schematic cross-section of the test module

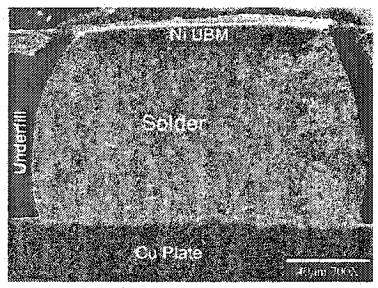


Figure 109 SEM secondary image of solder joint A on Module #3

Among the modules we tested, there are two different treatments of copper (Cu) plate surface: one with plated nickel barrier layer and one without. This difference is clearly shown under energy dispersive X-ray (EDX) analysis. An EDX Map can show the distributions of different elements on a surface. Figure 110 and Figure 111 show the EDX Map of a solder joint with nickel plate on top of the copper plate and a solder joint without nickel plate on top of the copper, respectively.

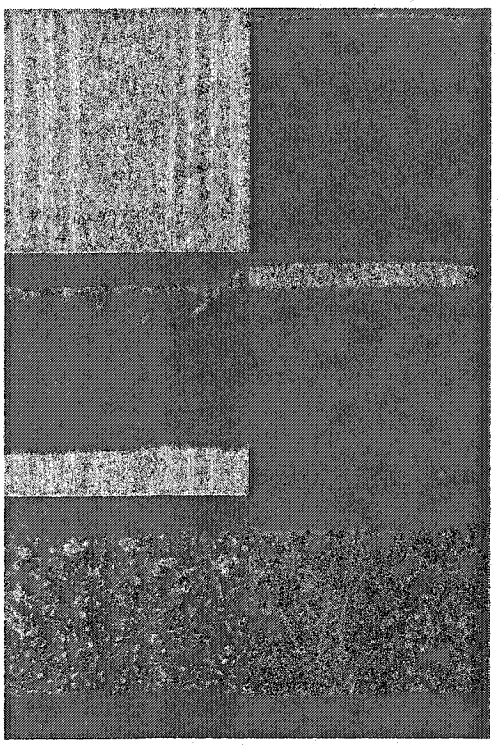


Figure 110 EDX Map for solder with Ni plate on Cu (from left to right and up to down: SEM, Al map, Cu map, Ni map, Pb map, and Sn map)

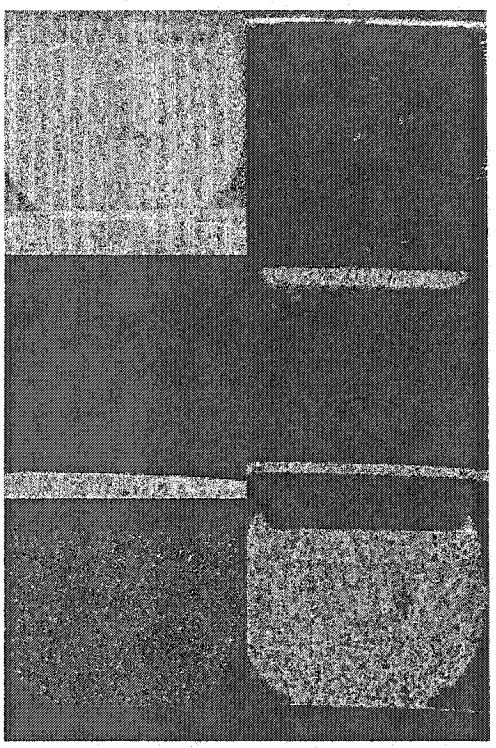


Figure 111 EDX Map for solder without Ni plate on Cu (from left to right and up to down: SEM, Al map, Cu map, Ni map, Pb map, and Sn map)

5.2.2 Calculation of cross section area of sectioned solder joint and current density

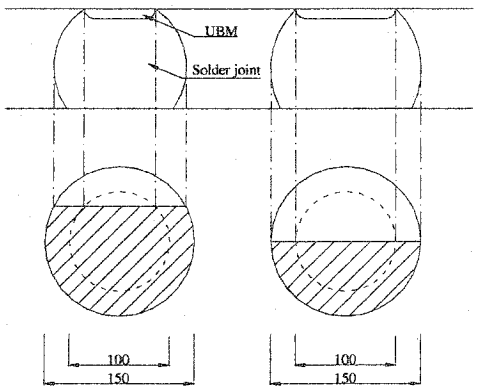


Figure 112 Schematic view of sectioned solder joint

Before the current stressing, each module is cross-sectioned with a precision diamond saw and then polished to expose the section of the solder joints. It is very

difficult to polish to the exact center of the solder joint (as shown in the right part of Figure 112) even if one checks the polishing progress constantly under a high power optical microscope. It is more likely that one will polish to somewhere near the center of the solder joint (as shown in the left part of Figure 112), but not the exact center. Thus the cross-section area (the shaded area in the Figure 112) of the solder joint subject to current stressing varies from solder to solder.

For the purpose of calculating the cross-section area of solder joint, the diameter of each solder joint is assumed to be 150μm, and the diameter of electroless Ni UBM on the Si die side is assumed to be 100μm. This may not be the case since it may vary from one solder joint to another due to manufacture imperfection. Based on this assumption, we can calculate the cross-section area (the shaded area in Figure 112) of each polished solder joint by measuring its width and the length of UBM on the polished surface. We can use this calculated cross-sectional area to compute the nominal current density for each solder joint in this chapter.

5.2.3 Electromigration Results

The test module was cross-sectioned and polished to the center of the solder joint using 240-, 600-, and 1200-grit silicon carbide abrasive paper. The joint was subjected to current stressing with 1 *Amp* DC under atmospheric ambient, yielding an average current density through the solder joint of 8×10^3 A/cm^2. The test module was taken off for scanning electron microscopy (SEM) analysis after 3, 6, 14.5, and 37.5 hours of stressing. A nano-indentation experiment was performed on the solder joint of Module # 1 after 37.5 hours of stressing.

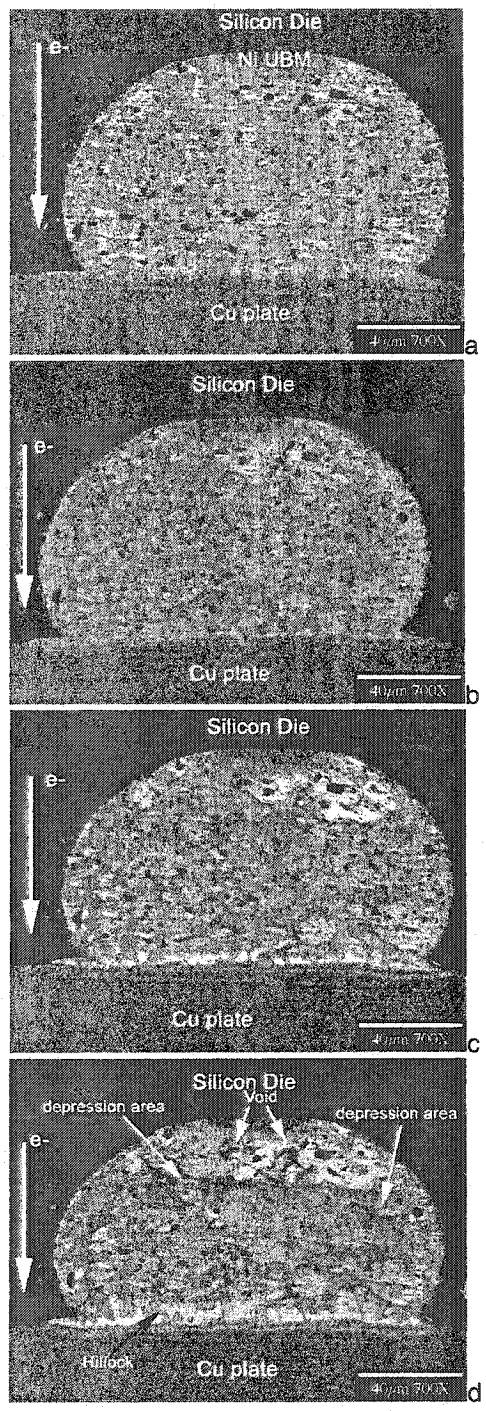


Figure 113. SEM backscattered image of solder joint on Module #1 for (a) initial, (b) 6 hrs, (c) 14.5 hrs, and (d) 37.5 hrs

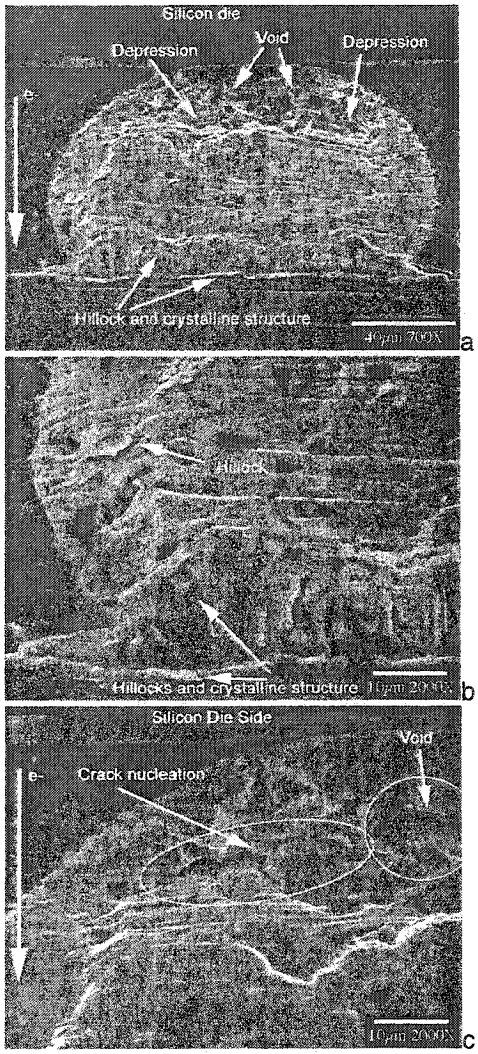


Figure 114. SEM secondary images for Module #1 (a) after 37.5 hours, magnification 700x (b) Area on the PCB board side (anode), 2000x; (c) Area on the silicon die side (cathode), 2000x.

The SEM backscattered images of the cross-sectioned surface of the solder joint are shown in Figure 113(a)-(d), for 0, 6, 14.5, and 37.5 hours of current stressing, respectively. SEM secondary images of the joint at several magnifications are shown in Figure 114(a)-(c) for 37.5 hours of stressing. The SEM backscattered image gives more information about elemental composition. On the SEM backscatter image, the light region corresponds to the Pb-rich region, and dark region corresponds to the Sn-rich

region because of their difference in elemental numbers. The secondary image gives more topographic information (Goldstern et al. 1992).

The direction of electron flow is from electroless Ni UBM on the silicon die side to the copper plate on PCB board side, or top to bottom in Figure 113. The mass accumulation on the anode side and the void nucleation on the cathode side can be seen in Figure 113 and Figure 114. The surface of the cross-sectioned solder joint became very rough after 37.5 hours due to electromigration. Large depression areas were formed on the cathode side and big voids formed near the electroless Ni UBM area, indicating a large amount of mass depletion in the region. Hillocks formed near the Cu plate region due to mass accumulation. Hillocks and crystalline formation are clearly shown in the anode region in Figure 114(a). Both voids and cracks can clearly be seen near the cathode region in Figure 114(c). It is worth pointing out that for a solder joint in real working condition, which would be surrounded by epoxy underfill, hillocks formation may be impeded. One can expect that much larger compression stress would develop in near anode region and tension stress would develop in near cathode region compared to the partially exposed cross-sectioned solder joint under test. The development of compressive and tensile stresses will in turn affect the rate of electromigration as in the case of thin film electromigration (Blech and Herring 1976).

5.2.4 Analysis of electromigration through marker displacement

In order to measure the atomic flux in the solder joint due to current stressing, inert particles on the sectioned solder surface were used as markers. The markers were SiC particles left on the surface during polishing. The Cu plate/solder interface was

chosen as the fixed frame of reference. This method was reported by Lee ,et al. in their electromigration experiment(Lee et al. 2001a). I will discuss later that this approach has weaknesses when thermomigration is signification during current stressing.

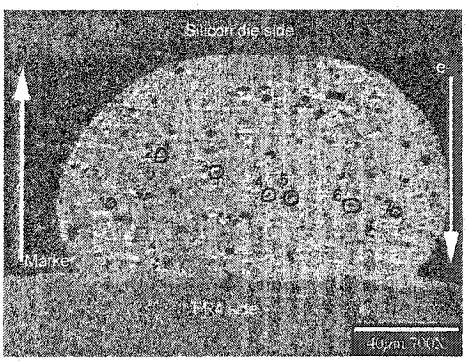


Figure 115. Markers position on the cross-sectioned surface (initial SEM backscatter image)

The markers position and their movements are shown in Figure 115 and Figure 116. All the markers have moved to the cathode side, which is the opposite direction of the electromigration flux. The measurement of marker movement was done by measuring the change in marker position with respect to the reference frame on the SEM backscatter images after 6, 14.5, and 37.5 hours of current stressing. The average movement of the markers, as the dashed line in Figure 117 shows, is a near linear dependence on current stressing time. This observation is consistent with Lee and Tu's observation (Lee and Tu 2001).

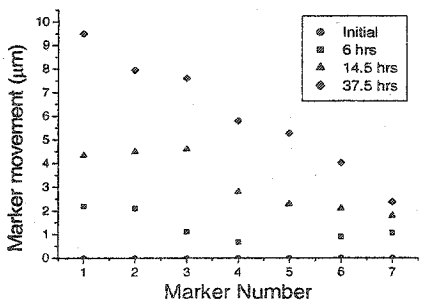


Figure 116. The marker movement on the sectioned eutectic SnPb surface

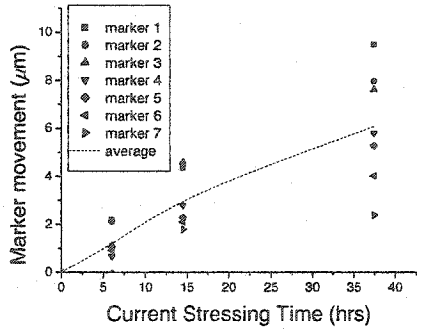


Figure 117. The marker movement vs. current stressing time.

Calculation of *DxZ in solder joint**

The atomic flux of electromigration can be calculated (Tu 1992a) from the marker movement, stressing time, and cross sectional area of solder at the initial marker position, using the following diffusion relation:

$$J_{atom} = \frac{V_{EM}}{\Omega \cdot A \cdot t} = C \frac{D}{kT} Z^* \cdot e \cdot \xi \qquad (5.1)$$

where

V_{EM} = the volume of solder moved by electromigration, cm^3.

Ω = the average atomic volume of the solder, $cm^3 / atom$.

A = the cross sectional area at the initial marker position, cm^3.

t = the time of current stressing, *seconds*.

C = the number of atoms per unit volume, $atoms / cm^3$ (assumed to be $1/\Omega$ in a unary system).

D = the diffusivity, $cm^2 / second$.

$k = 8.617 \times 10^{-5} eV / K$ (the Boltzman's constant).

T = the temperature in Kelvin.

Z^* = the effective charge number.

e = the electron charge.

ξ = the electrical field, $Volt/cm$.

The volume of solder moved by electromigration, V_{EM}, is calculated from the average marker movement (Lee et al. 2001a). In this experiment, the V_{EM} is calculated to be $4.51\text{x}10^{-8}\,cm^3$ after 37.5 hrs of current stressing. The cross-sectional area of the solder joint at the initial marker position is $7.697\text{x}10^{-5}\text{cm}^2$. The average marker movement is $6.078\mu m$. The electrical field is calculated with a eutectic SnPb solder resistivity of $15\mu\Omega\cdot cm$ at room temperature and the current density is calculated from the measured current and the cross-sectional area of solder joint at the initial marker position. In this experiment, the stressing current is $1Amps$ so that the current density is $1.3\text{x}10^4 A/cm^2$ and the electrical field $\xi = \rho j = 15\times10^{-6}\times1.3\times10^4 = 0.195V/cm$.

Table 8 Comparison of DxZ^*

	Lee et al.'s(Lee et al. 2001a)	Lee & Tu's (Lee and Tu 2001)	Present study
Temperature(°C)	120	120	Atmospheric ambient
Current Density (A/cm^2)	$2\text{x}10^4$	$3.8\text{x}10^4$	$1.3\text{x}10^4$
Time (hrs)	324	39.5	37.5
DXZ^*	$2.16\text{x}10^{-11}$	$1.85\text{x}10^{-10}$	$5.62\text{x}10^{-10}$

The value of DxZ^* is thus computed and compared to Lee et al.'s and Lee and Tu's test results(Lee and Tu 2001), as shown in Table 8. It shows the values of DxZ^* are different between Lee et al.'s as well as Lee and Tu's experiments and the present one. The reason for the difference will be discussed in the later section after we discussed the the observation of thermomigration due to joule heating in flip-chip solder joints during current stressing.

5.2.5 Discussions

In this section, a preliminary test was conducted to study the effects of high current stressing on a very small flip-chip solder joints. Using SEM, microstructural evolution was monitored. Through analysis of the movement of markers during current stressing, the atomic flux is obtained. As a preliminary test, several problems were identified and revised test procedures were applied in the later experiments. First, only solder joint A was analyzed in the experiment, although there were two solder joints under current stressing in Module #1. Since the direction of electric current in solder joint B is opposite to that in solder joint A, it is of research interest to see the effect of current direction. In later experiments, both solder joints are subjected the same test procedures. Second, the stressing temperature of the solder joint was not measured in the experiment. At the time, we thought that the stressing temperature of solder joint is not far from atmosphere ambient temperature as assumed by Lee et al.(Lee et al. 2001a). We later found that the stressing temperature, in solder joint due to Joule heating can be much higher than ambient temperature. An Omega® HH-602 K type thermocouple thermometer is used to measure the temperature on silicon die during current stressing after we noticed this fact in the later experiments.

5.3 Thermomigration under Joule Heating during Current Stressing

In this section, thermomigration due to the thermal gradient in the solder joint caused by joule heating is reported. A three dimensional coupled electric thermal finite element (FE) simulation of a realistic flip-chip module shows the existence of thermal gradient in the solder joint which is high enough to trigger thermomigration.

5.3.1 Introduction

During current stressing, heat is also generated due to joule heating in the flip-chip module. In a typical flip-chip module, the cross-section area of the metal trace on the silicon dies is much smaller than that of the solder joint. Thus the primary heat source is the metal trace, which contributes to the most of the electric resistance of the module. Current crowding also contributes to the uneven local joule heating. The joule heating during current stressing may maintain a thermal gradient in the solder joint. Lee et al.(Lee et al. 2001a) conducted electric current stressing test on flip-chip solder joints and concluded that thermomigration is not a dominant mechanism. But their methodology used to draw this conclusion is questionable. They used a similar test module where there were two solder joints (solder joint A and solder joint B as defined in Section 5.2) under stressing. They only sectioned and monitored solder joint A during current stressing and observed severe migration in that solder joint. After stressing, they then sectioned solder joint B and observed no migration at all. Therefore, they argued that since both solder joints were subjected to the same temperature gradient, solder joint B should have the same diffusion profile as solder joint A if thermomigration is dominant. But the fact is that the sectioning and polishing after stressing on solder joint B may well eliminate any evidence of migration in this solder joint. They used melting crayon to monitor the temperature of the solder joint, which is not a reliable way. In our revised test procedures, both solder joints were monitored during current stressing.

Thermal migration is reported in Pb-In solder alloy at a thermal gradient of $1200^{o}C/cm$ by Roush et al (Roush and Jaspal 1982). A three dimensional coupled thermal electrical FE simulation on a realistic flip-chip module is performed, and the result shows

that a thermal gradient greater than Roush's reported value is possible in the solder joint. The measured temperature on the silicon die agrees with that from the FE simulation. In some cases, void nucleation is observed near the anode side in some solder joints, which can not be explained by electromigration. In these cases, the anode side is also the hotter side (silicon die side). The authors believe thermomigration (in the opposite direction of electromigration) is dominant in these cases.

5.3.2 Experiment results

Figure 118 show the secondary SEM images of solder A and solder B from Module #14 after 16 hours of 1*A* current stressing. The calculated current density in the solders is about $1.3\times10^4 A/cm^2$. Severe void nucleation is observed on solder A near the Si die side (which is also the cathode). This is as expected since the direction of electromigration is from cathode to anode. Hillocks are observed near the Cu plate side or the anode side on solder A. Void nucleation is also observed on solder B near the Si die side which is the anode side. Although the void nucleation on solder B near the Si die side is much less severe compare to that on solder A, electromigration alone can not explain this observation. If electromigration were the only driving process in microstructure evolution of solder during current stressing, void nucleation should be expected to start near cathode side, e.g. the Cu plate side for solder B, which was not the case. Similar observations were found on several other test modules, as shown in Figures 119-125. In these modules, the stressing current range is between 0.9~1A. The calculated current density ranges from $0.6\sim1.1\times10^4 A/cm^2$. Therefore, there has to be another process operative during the current stressing.

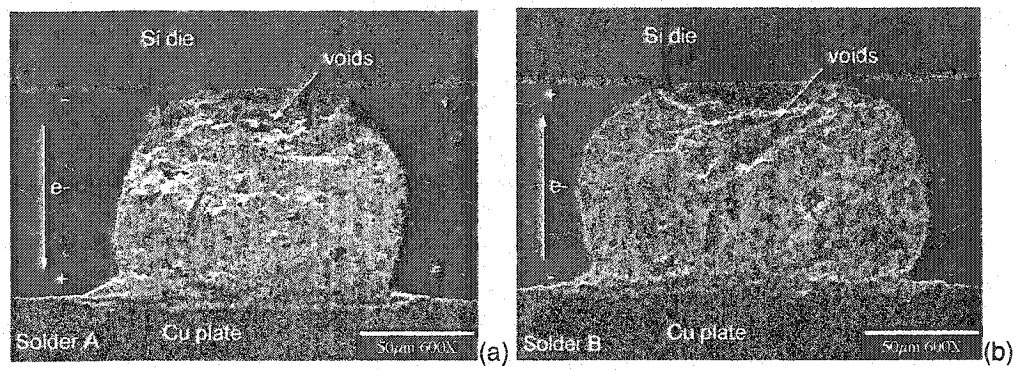


Figure 118 Secondary SEM of (a) solder joint A ($1.2\times10^4 A/cm^2$); (b) solder joint B ($0.9\times10^4 A/cm^2$) on Module #14 after 16 hrs 1A stressing

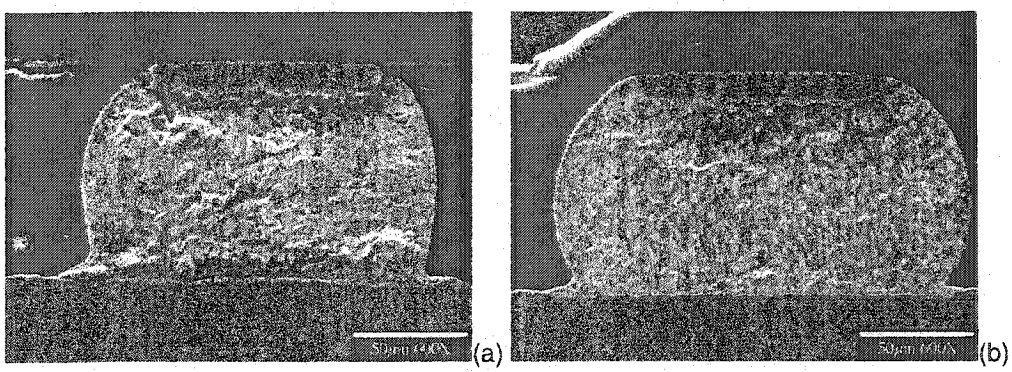


Figure 119 Secondary SEM of (a) solder joint A ($1.13\times10^4 A/cm^2$) (b) solder joint B ($0.88\times10^4 A/cm^2$) on Module #12 after 36 hrs 1A stressing

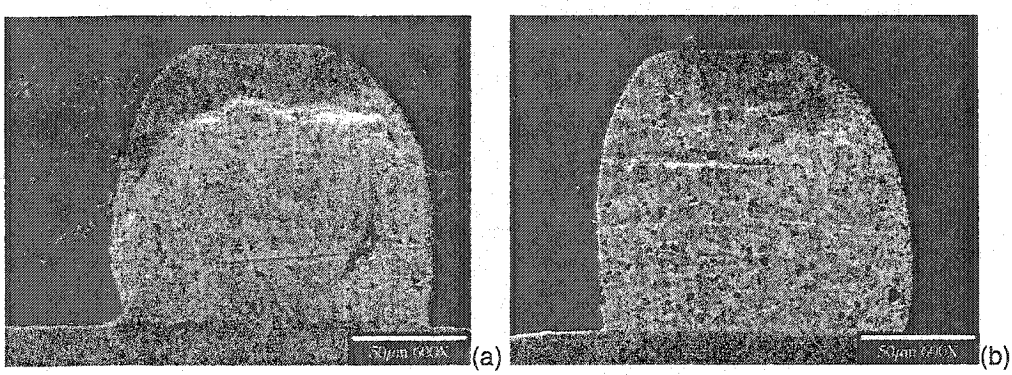


Figure 120 Secondary SEM of (a) solder joint A ($0.62\times10^4 A/cm^2$) (b) solder joint B ($0.61\times10^4 A/cm^2$) on Module #34 after 865 hrs 0.9A stressing

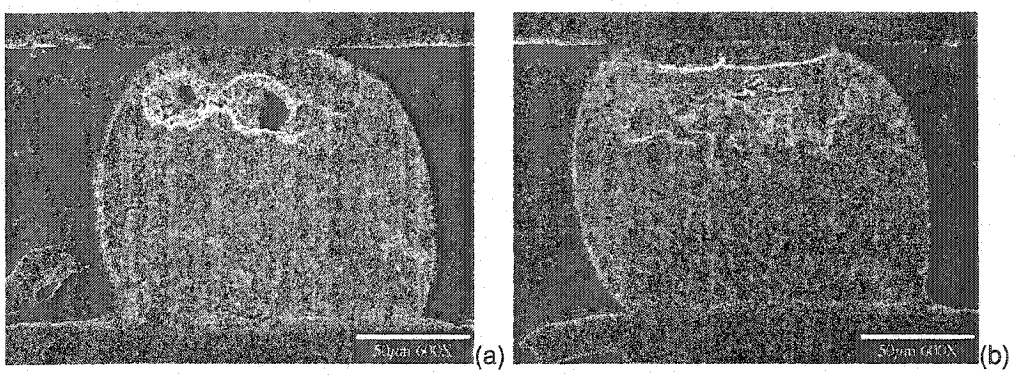


Figure 121 Secondary SEM of (a) solder joint A ($0.96\times10^4 A/cm^2$) (b) solder joint B ($1.0\times10^4 A/cm^2$) on Module #41 after 60 hrs 1A stressing

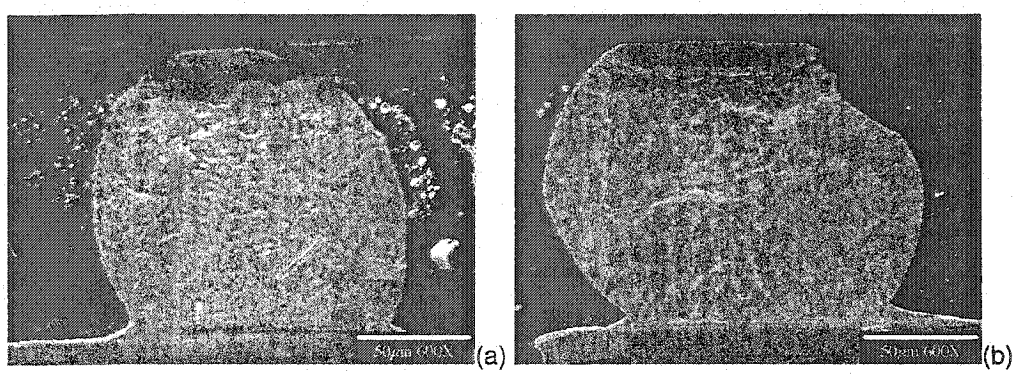


Figure 122 Secondary SEM of (a) solder joint A ($0.72\times10^4 A/cm^2$) (b) solder joint B ($0.73\times10^4 A/cm^2$) on Module #42 after 129 hrs 1A stressing

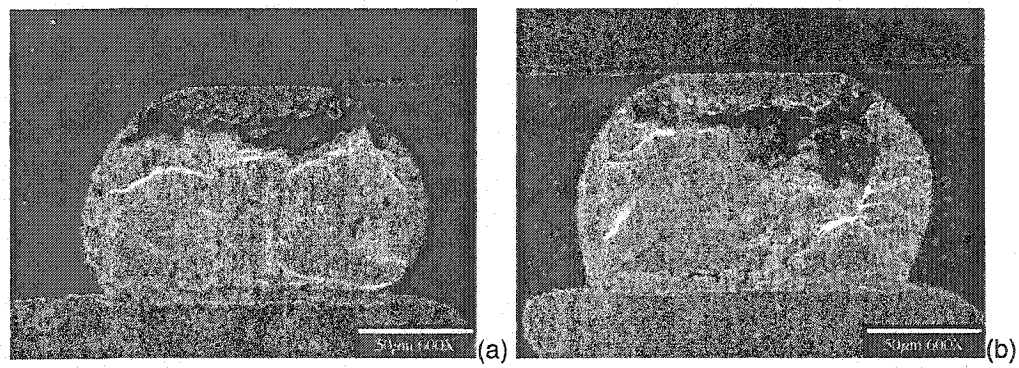


Figure 123 Secondary SEM of (a) solder joint A ($0.64\times10^4 A/cm^2$) (b) solder joint B ($0.68\times10^4 A/cm^2$) on Module #51 after 168 hrs 1A stressing

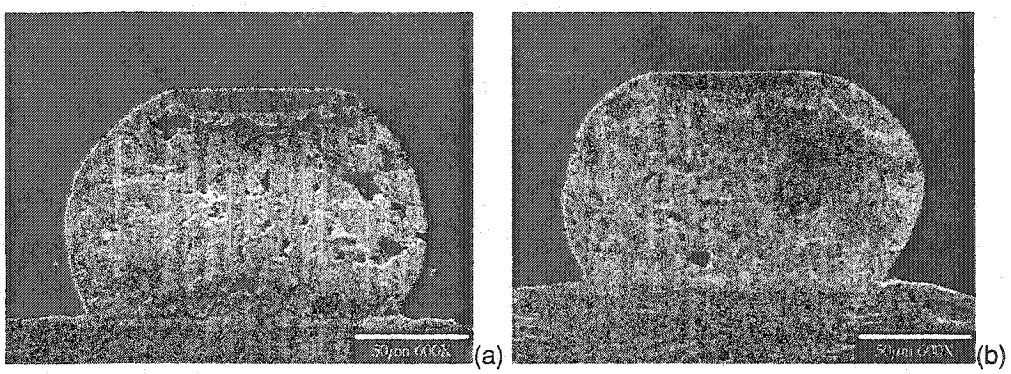


Figure 124 Secondary SEM of (L) solder joint A ($0.71\times10^4 A/cm^2$) (R) solder joint B ($0.68\times10^4 A/cm^2$) on Module #52 after 590 hrs 1A stressing

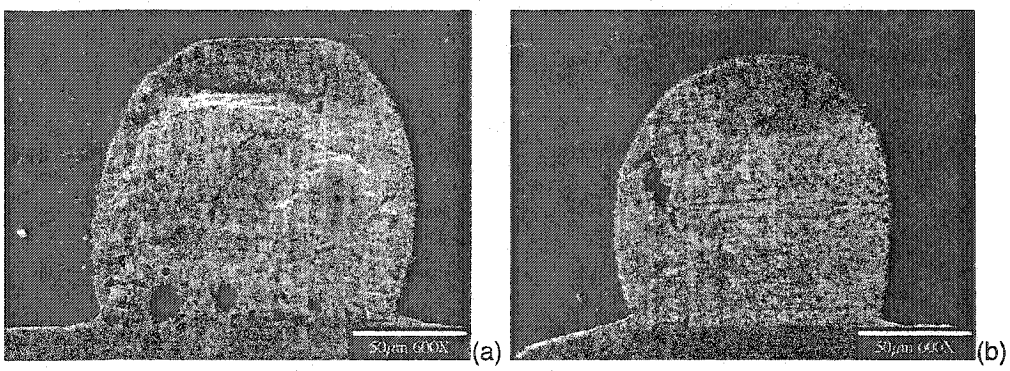


Figure 125 Secondary SEM of (a) solder joint A ($0.68\times10^4 A/cm^2$) (b) solder joint B ($0.64\times10^4 A/cm^2$) on Module #56 after 932 hrs 1A stressing

We think this process is thermomigration. Since the Al trace on the Si die contributes to the most of the electrical resistance, most of the joule heating is generated in Al, which makes the silicon die side very hot. During the experiments, the temperature on top of the silicon die measured by a thermal couple ranged from $40\sim200^oC$ for different modules under different current stressing level. Thus it is reasonable to assume that there is a temperature gradient maintained in the solder joint during current stressing. This assumption is verified by a three dimensional coupled thermal electrical FE simulation of the test module, as will be reported in the next section. Thermomigration would start in the solder joint with the existence of a thermal gradient. Roush et al.(Roush and Jaspal 1982) observed the thermomigration of Pb/In solder alloy at a thermal gradient of $1200^oC/cm$ and reported that both In and Pb move in the direction of the thermal

gradient. Van Gurp et al.(Van Gurp et al. 1985) reported fast thermomigration in In and In alloy films and found that material is transported from hot to cold areas. Thermomigration in pure Pb has been observed by Johns et al.(Johns and Blackburn 1975) over the temperature range 322~202 ^{o}C. They reported that in all circumstances, flow of material was from hot to cold. In our experiments, thermomigration in eutectic Pb/Sn solder is from the hot side (Si die side) to the cold side (Cu plate side), which agrees with above reports. Thermomigration may assist electromigration if the hot side coincides with the cathode side, as in solder A, or it may counter electromigration if the hot side coincides with anode side, as in solder B. If thermomigration outbalances electromigration in the overall diffusion process during current stressing in the latter case, void nucleation would be found near anode side, as are the cases in Figures 118(b)-125(b). Thermomigration can also explain our observation that much more severe voids formed near the Si die side in solder A than in solder B. This conclusion suggests that thermomigration may not be omitted in the electromigration analysis of flip-chip solder joint when joule heating from Si die is not negligible.

Besides the observation of void nucleation near the anode side in solder B, inert marker movements also suggest mass flow in the opposite direction of electromigration on solder B on some test modules. SiC particles left on the surface during polishing can be used as inert marker to measure the atomic motion in solder joint(Lee et al. 2001a). Figure 126 shows the measurement of marker movement on solder B on Module #14 as shown in Figure 118. The inert markers are expected to move in the opposite direction of electromigration (Lee et al. 2001a), as shown in Figure 126, or from the Si die side to the Cu plate side, as in solder B. Figure 127 shows the marker movement vs. stressing time,

which indicates markers actually moved in the same direction as electromigration (as indicated by the negative values). This observation suggests that the actual overall diffusion direction is from the Si die side (hot side and anode side) to the Cu plate side, indicating the influence of thermomigration during current stressing. The measured marker movement on solder A of the Module #14 shows the mass diffusion from the Si die side (hot side and cathode side) to the Cu plate side, but with a higher value since thermomigration assisted electromigration in solder A.

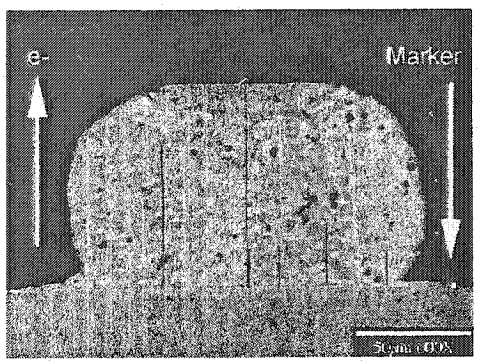


Figure 126 Marker measurement on Solder B of Module #14

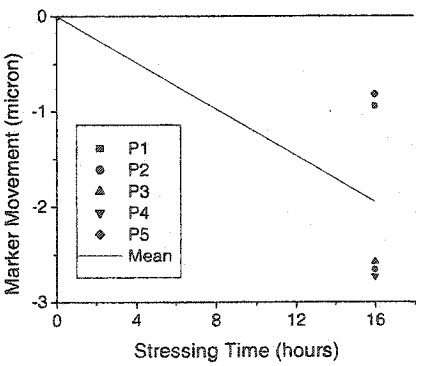


Figure 127 Marker movement vs. stressing time on solder B of Module #14

Assuming that the metal atoms migrate via a vacancy diffusion mechanism, the flux of metal atoms is equal and opposite to the flux of vacancies. Following Kirchheim (Kirchheim 1992), the flux of vacancy in a metal due to electron wind force is:

$$\vec{q}_{em} = -\frac{D_v C_v}{kT} Z^* e \vec{\nabla} \Psi , \tag{5.2}$$

where D_v is vacancy diffusivity, C_v is vacancy concentration, k is Boltzman's constant, Z^* is vacancy effective charge number, e is electron charge, Ψ is electric potential field. The flux of vacancy due to spherical stress gradient by Kirchheim (Kirchheim 1992) is:

$$\vec{q}_{\sigma} = -\frac{D_v C_v}{kT} f \Omega \vec{\nabla} \sigma , \tag{5.3}$$

where f is vacancy relaxation ratio, Ω is atomic volume. If there exists a thermal gradient in the metal, the flux due to thermomigration by Huntington (Huntington 1972) is:

$$\vec{q}_{th} = -\frac{D_v C_v}{kT^2} Q^* \vec{\nabla} T , \tag{5.4}$$

where Q^* is heat of transport, the isothermal heat transmitted by the moving atom in the act of jumping, less its intrinsic enthalpy. By combining all the above flux components plus the flux generated by the vacancy concentration gradient, the total vacancy flux in a metal under current stressing is thus:

$$\vec{q} = -D(\vec{\nabla} C + \frac{C}{kT} Z^* e \vec{\nabla} \Psi + \frac{C}{kT^2} Q^* \vec{\nabla} T + \frac{C}{kT} f \Omega \vec{\nabla} \sigma). \tag{5.5}$$

This diffusion flux equation is the one that we have used in the numerical simulations in Chapter 4, although there is no thermal gradient in the simulations. It shows that if thermal gradient is not negligible, thermal migration may assist or counter electromigration diffusion depending on the directions of electric gradient and thermal gradient.

It is clear that in the presence of thermomigration, Equation (5.1) cannot be used to extract effective charge number. Therefore, although marker movement can be used to estimate the atomic flux in solder joint during current stressing, it cannot be used to

extract the information on effective charge number because of multiple field forces. This finding explains the discrepancy of effective charge number between our results and those in the literature, as shown in Table 8. The magnitude of thermomigration is related to the thermal gradient within the solder joint, which is dependent on the testing ambient temperature and the thermal management of the test module.

5.3.3 Coupled thermal-electrical FE simulation

A three dimensional coupled thermo-electrical FE simulation of the real structure of a flip-chip test module is conducted to determine the temperature distribution in the solder joint. Abaqus is used as the finite element code. Since in the experiment the module was cross-sectioned, only a cross-sectioned module is modeled. In the simulation model, the thickness of the Al trace is $1\mu m$ and the width is $150\mu m$. It connects two solder joints as shown in Figure 112. The solder joint has a diameter of 150 μm and a height of 100 μm. Due to the symmetric geometry of the module, only half of the module is modeled. Joule heating due to electric current is the only thermal loading applied on the system. The thermal boundary condition is that the temperature on the far end surface of the PCB is fixed at room temperature ($23^{o}C$). The thermal radiation is considered for all the external surface of the module and an emissivity of 0.7 is assumed. The electric potential is fixed to be 0 at one end of the Al trace and a concentrated current load is applied at the other end of Cu plate. The material properties used in the simulation are taken from Pecht et al. (Pecht et al. 1998), as shown in Table 9.

Table 9 Material properties (Pecht et al. 1998)

	Thermal conductivity ($w/cm\text{-}C$)	Electric conductivity ($ohm^{-1}\text{-}cm^{-1}$)	Density (g/cm^3)	Thermal Capacity ($J/g\text{-}C$)
Al	2.37	3.1×10^{5}	2.7	0.894
Cu	4.03	4.89×10^{5}	9	0.385
FR4	0.015	5×10^{-14}	2.54	1.0
Si	1.5	1.56×10^{-5}	2.3	0.712
Solder	0.506	6.9×10^{4}	8.48	0.134
Underfill	0.03	1×10^{-14}	1.15	1.6

The mesh used for simulation is shown in Figure 128. Figure 129 shows a close look at the mesh for the region of solder joint.

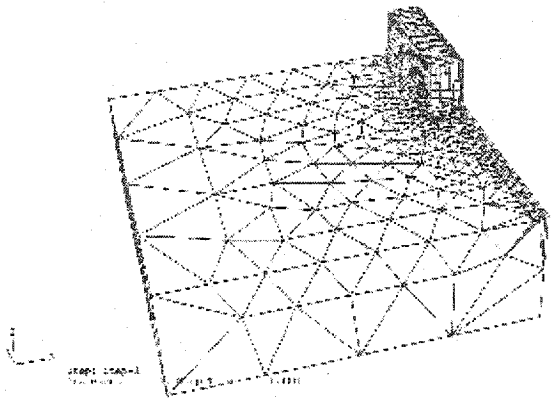


Figure 128 Mesh of the simulation model

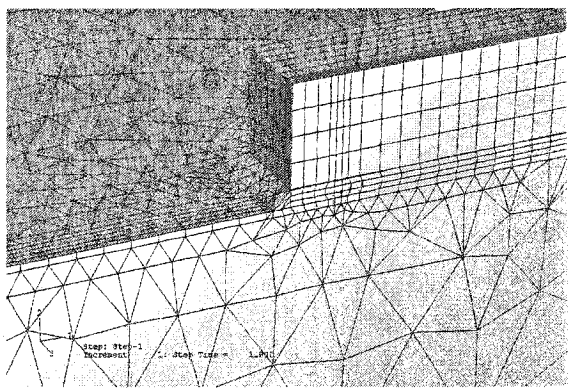


Figure 129 Mesh of the simulation model – region of the solder joint

Three electrical loading cases were considered in the simulation: $1A$, $0.8A$, and $0.6A$. The temperature distribution for the case of $1A$ current loading is shown in Figure 130. The Al trace and Si die has the highest temperature ($150^{o}C$), which agrees with the measured temperature in the test. The temperature distribution on the solder joint alone is

shown in Figure 131. Figure 132 shows temperature gradient through a vertical line across the solder joint. A thermal gradient of $1500^{o}C$/cm is predicted in the simulation, which exceeds the thermal gradient reported by Roush. The real temperature gradient in the solder joint may not be exactly $1500^{o}C$/cm due to the discrepancies between the simulation model and the real module. This simulation just verifies the existence of a great thermal gradient in solder joint to trigger thermomigration during current stressing.

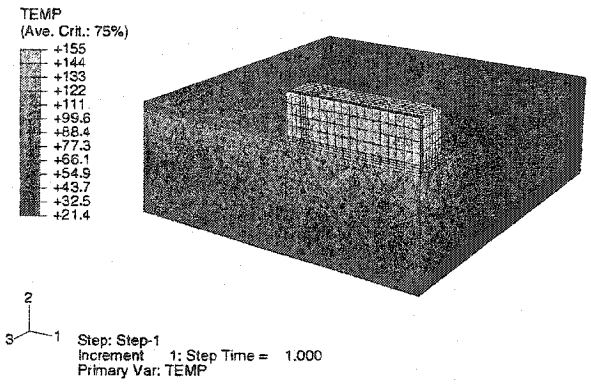


Figure 130 Temperature distribution on the module for loading case of 1*A*

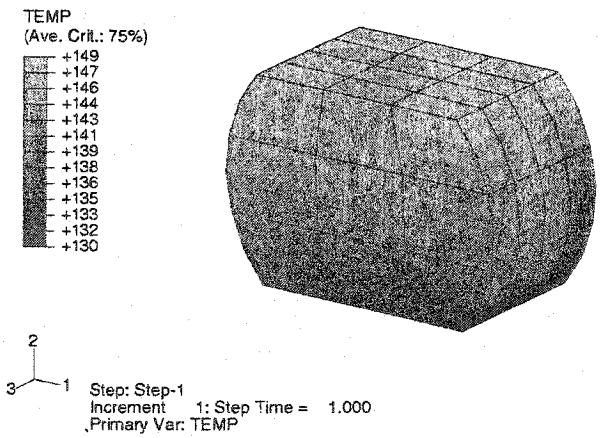


Figure 131 Temperature distribution on the solder for loading case of 1*A*

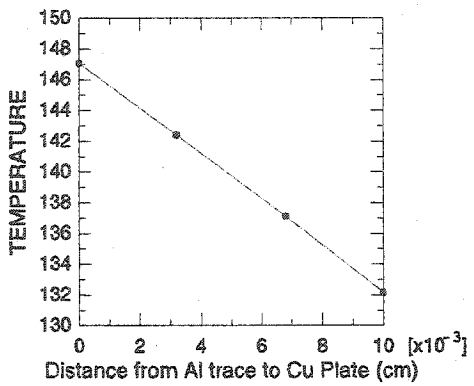


Figure 132 Temperature distribution along the vertical line across the solder for loading case of 1A

The temperature distribution on the module for the loading case of 0.8A is shown in Figure 133. Figure 134 and Figure 135 show temperature gradient through a vertical line across the solder joint for the loading case of 0.8A and 0.6A, respectively. It is clearly shown that in both cases a temperature gradient ($1000^{o}C$/cm for loading case of 0.8A and $500^{o}C$/cm for loading case of 0.6A) is maintained in the solder joint during electric current stressing. Compared to the case of 1A current loading, it is clear that higher stressing current levels lead to higher temperature gradients as well as higher absolute temperature within the solder joint. Therefore, a flip-chip solder joint subjected to higher current level is likely subjected to more severe thermomigration in addition to electromigration. This observation further indicates that by using proper thermal management to reduce the temperature gradient in flip-chip solder joints, thermomigration can be greatly reduced and therefore the reliability of solder joint can be greatly improved.

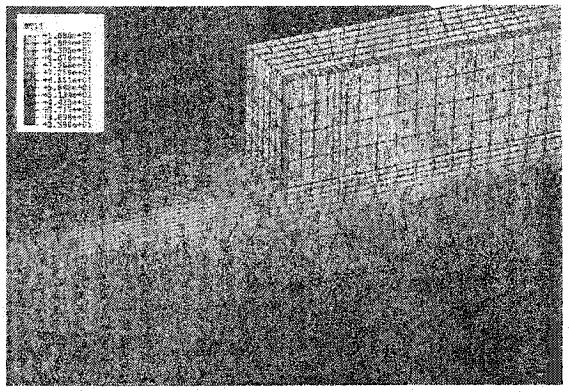


Figure 133 Temperature distribution on the module for loading case of 0.8*A*

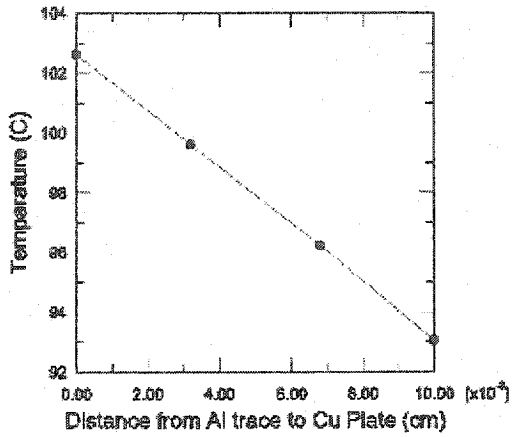


Figure 134 Temperature distribution along the vertical line across the solder for loading case of 0.8*A*

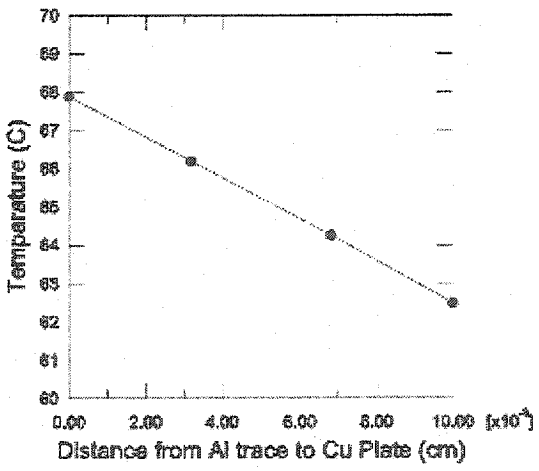


Figure 135 Temperature distribution along the vertical line across the solder for loading case of 0.6*A*

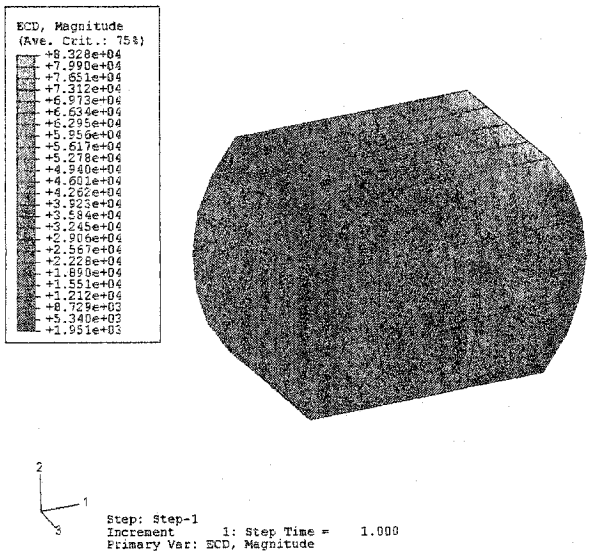


Figure 136 Current density distribution in the solder joint for loading case of 0.8*A*

Figure 136 shows the electric current density distribution in the solder joint for the loading case of 0.8A. Current crowding is clearly shown in the upper-right region of the solder joint.

5.3.4 Conclusions

Thermomigration of flip-chip solder joints under current stressing is reported in this section. The authors believe that the joule heating from the silicon die maintains a significant thermal gradient within the solder joint, which triggers thermomigration. An FE simulation result supports the existence of the thermal gradient. Thermomigration may assist or counter electromigration depending on the direction of the thermal gradient and electric field. Besides electromigration, thermomigration is also a reliability concern for flip-chip solder joints under high current stressing. A governing vacancy diffusion equation for both electromigration and thermomigration is proposed. By extending the Sarychev constitutive model to the case of thermomigration, the stress evolution under

both electromigration and thermomigration can be obtained by solving the coupled diffusion-mechanical partial differential equations.

Since the thermomigration is of the same magnitude of electromigration, the methodology of using inert marker movement to estimate the product of effective charge number and diffusivity is no longer valid. Although marker movement can still be used to estimate the atomic flux, this atomic flux is now viewed as the combination of electromigration and thermomigration. Based on this finding, the calculation of the product of effective charge number and diffusivity is not presented except for Module #1.

5.4 Failure Modes of Flip-chip Solder Joints under Current Stressing

In this section, the failure modes of flip-chip solder joints under current stressing are analyzed based on the experiments of 20 flip-chip modules. Three different failure modes were reported. Among them, only Mode 3 failure is caused by the combined effect of electromigration and thermomigration, where void nucleation and growth contribute to the ultimate failure of the module. The void nucleation and growth in solder joint during current stressing is discussed in detail. The Ni UBM-solder interface is found to be the favorite site of void nucleation and growth. The effect of pre-existing voids on the failure process of a solder joint is found to be dependent on their location. The time to failure of the test modules is found to generally obey Black's law but with some exceptions. The exceptions are due to the different failure mechanism in these test modules.

5.4.1 Introduction

The research on electromigration in solder joints is still rudimentary. The failure modes of flip-chip solder joints under high electric current stressing is not yet well understood. In the experiments, 20 test flip-chip modules were subjected to DC electric current stressing. The stressing current levels range from 0.5 to 1.5A and lead to a current density in the solder joint from 0.4 to 1.2 × 10^4A/cm^2, which is dependent on the cross-sectional area of solder joint. Two test modules were subjected to DC pulse current stressing at a level of 3~10A. Fourteen test modules failed due to current stressing, four test modules were damaged due to re-polishing after the nano-indentation test, and two test modules survived after more than 3000 hours of stressing and did not fail. Table 10 shows the test matrix of the experiment. In this section the module names are simplified as M1, M2, etc., where M1 stands for Module #1.

Table 10 Test matrix of flip-chip modules

Current level	Test module
0.5A	M8, M15, M26
1A	M1, M6, M12, M14, M31, M33, M41, M42, M51, M52, M54, M56
0.9A	M34
1.15A & 1.5 A	M5, M53
Pulse	M4, M7

5.4.2 Failure modes of test modules

Of the 14 modules that failed due to electrical current stressing, three types of failures were observed in our experiments: 1) failure due to melting of solder; 2) failure in the Al trace; 3) failure due to void nucleation and growth in the solder joint during current stressing.

The reason for the first type of failure is obvious since the Pb/Sn eutectic solder has a low melting point of 183°C. M31, M33, and M53 had this type of failure. M31 and M33 failed after 30 minutes of current stressing with a measured Si die temperature of over 200°C. The solder joints in these two test modules melted. The heat in M31 was apparently generated in the Al trace since the solder joints have good wetting with both Ni UBM on the Si die side and Cu plate on the FR4 side. Therefore, Al trace contributed to most of the resistance. The heat in M33 might have come from both the Al trace and solder joint A, since solder joint A apparently had very bad wetting with the Cu plate, as shown in Figure 137. For M31 and M33, electromigration and thermomigration should have no contribution to the failure of the module. M53 survived just 22.5 hours of current stressing. The initial stressing temperature measured on the Si die was first 150°C then gradually raised over 180°C. Figure 138 shows that even half an hour before the final failure, solder joint A melted. Figure 138 also shows a misregistration of solder joint B in Module 53. Thermomigration is clear in solder B, as large voids were observed in solder joint B near the Ni UBM-solder interface (as discussed in Section 5.3). Since the temperature measured on the silicon die was so high, an extremely high thermal gradient might be maintained in the solder joints to trigger thermomigration, as predicted by the 3-D coupled thermal-electrical FE simulation.

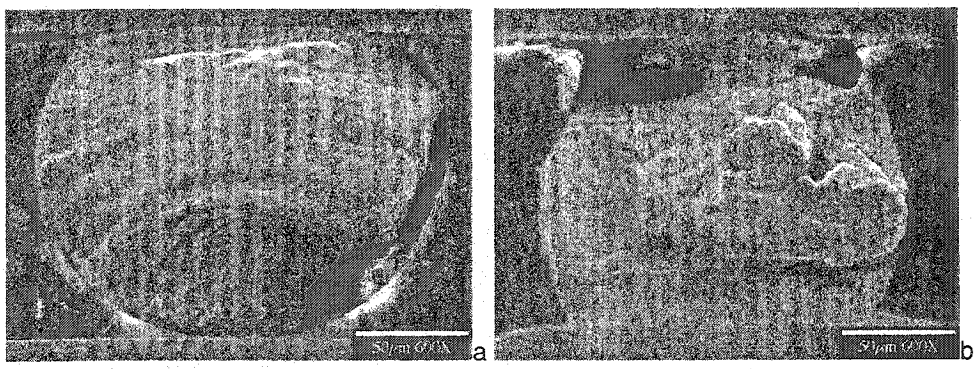


Figure 137 Secondary SEM of M33 after failure (a) solder joint A (b) solder joint B

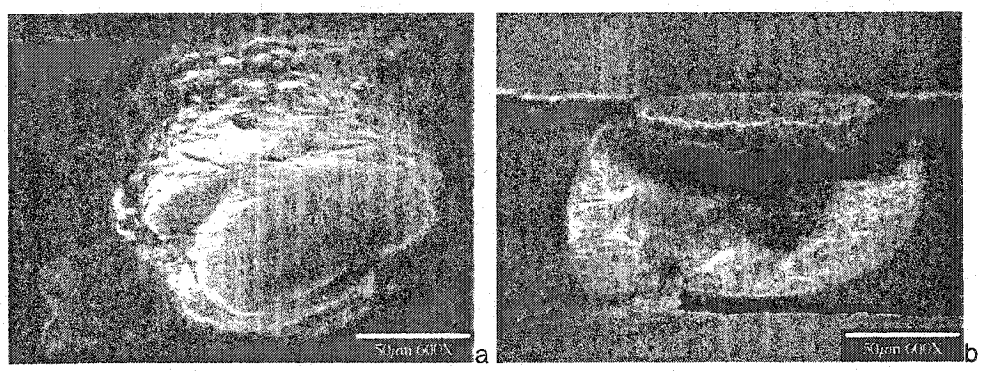


Figure 138 Secondary SEM of M53 after failure (a) solder joint A (b) solder joint B

M4, M5, M7, and M54 were subjected to Type 2 failures. M4 and M7 were subjected to pulsed direct current (PDC) stressing instead of continuous current stressing. Tektronix ® 371A programmable high power curve tracer was used for pulse stressing. The pulse frequency is 120 Hz, with a pulse width of ~80 micro seconds. Pulse shape depends on the wiring impedance, but resembles a rectangular wave. The duty factor (defined as the ratio of time of the on period to that of the whole pulse period) is calculated to be 0.96%. When M4 was subjected to 10A peak PDC stressing, its resistance immediately increased to infinity. The SEM image shows that the damage of the module was in the Al trace and the silicon die as clearly shown Figure 139(a). M7 was first subjected to 3A of PDC stressing for 50 hours, then 5A of PDC stressing for 57 hours, and finally 7A of PDC stressing for 23 hours. SEM images taken after stressing shows that there were no microstructural change or void nucleation in the solder joints at

all. When M7 was subjected to 10A of PDC stressing, it failed immediately. Figure 139(b) shows that the Al trace was the actual cause of the failure.

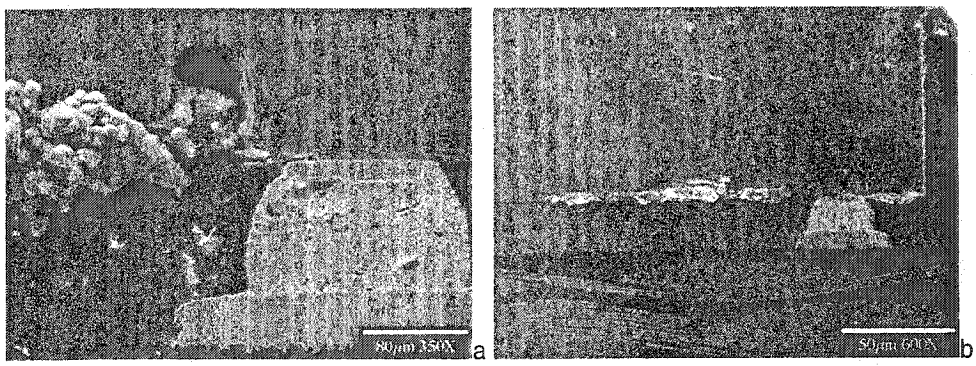


Figure 139 Failure in the Al trace and Si die (a) M4, solder joint A (b) M7, solder joint A

With 7A of PDC, the peak current density in the solder joints was $5\sim7\times10^4$A/cm^2 and the peak current density in the Al trace was 7×10^6A/cm^2. This is much higher than that applied in the continuous dc current stressing experiments. The effect of PDC on electromigration has been shown to be dependent on the frequency and duty factor (Li et al. 1999). At low frequencies electromigration acts as if it were dc for the time 'on' and back diffusion may occur during the time 'off' (Lloyd 1999b). In our experiment, the PDC frequency is within the low frequency range. The reason that we did not observed any damage in the solder joint during PDC stressing even though very high current density was applied may be due to the low duty factor (0.96%) of PDC. The low duty factor has two effects on electromigration. First, the joule heating generated in the Al trace during time 'on' is readily dissipated before it transfers to the solder joints, therefore the temperature on the solder joints during the whole pulse period is low (close to ambient). The low temperature also leads to a low diffusivity of solder which makes the solder joint less prone to migration. Second, the low duty factor means less accumulated 'on' time and more 'off' time for back diffusion. The accumulated 'on' time

of M7 during its 130 hours of PDC stressing is about 1.3 hours. On the other hand, high peak current of PDC generates a lot of heat in the Al trace, which leads to its failure.

M5 and M54 also experienced Type 2 failure although they were subjected to dc stressing. The applied current on M5 was 1.5A and the module immediately failed. SEM secondary images of the solder joint B before and after stressing are shown in Figure 140. Figure 140(b) shows that Si die was separated from the solder joint and underfill along the Al trace where tremendous heat was generated. When 1A of dc current was applied to M54, the resistance of the module immediately increased from 1.6Ω to 9 Ω. There were no microstructural change or void nucleation on the solder surface after the failure of module, as shown in Figure 141. The failure is in the Al trace. The initial module resistance of 1.6Ω (comparing to 0.4~0.6Ω) indicates the Al trace might have been partially damaged due to the polishing process and can be easily damaged by the electric current of 1A.

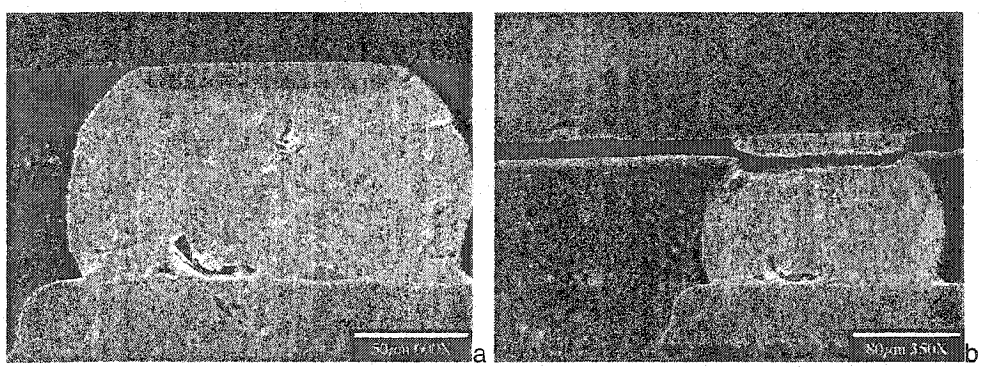


Figure 140 Secondary SEM of M5, solder joint B (a) initial (b) after failure

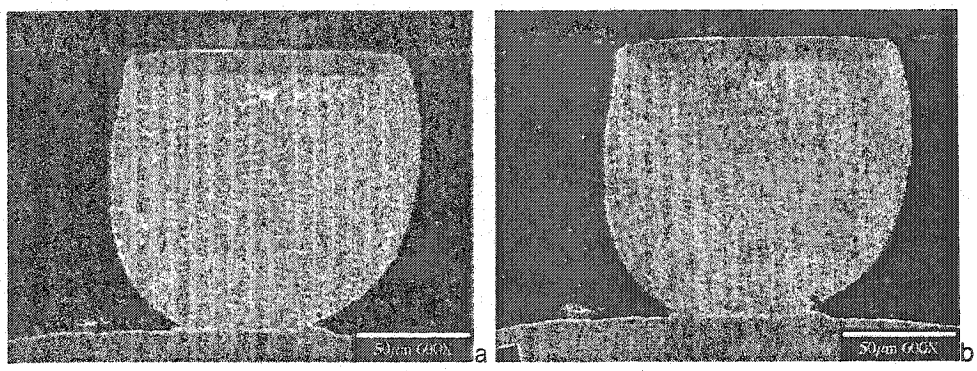


Figure 141 Secondary SEM of M54, solder joint B (a) initial (b) after failure

M6, M14, M34, M41, M42, M51, and M56 were subjected to Type 3 failure - due to void nucleation and growth in the solder joints under current stressing. In these modules, severe void nucleation was observed in the solder joints before the failure of the modules. The fact that void nucleation was always on Si die side and mass accumulation on the Cu plate side of the cross-sectioned solder surface indicates that the failure process in solder joint is the combined effect of electromigration and thermomigration, as shown in Figure 142. In these modules, solder joint A (where the direction of electromigration is the same as that of thermomigration) always had much more severe void nucleation than solder joint B (where the direction of electromigration is opposite to that of thermomigration). Therefore, I think that it was the degradation of solder joint A that caused the ultimate failure of the module under current stressing. Unlike to Type 3 failure, Type 1 and Type 2 failures are not due to electromigration or thermomigration in solder joints, since there was no time for the migration to happen before the module failed due to other causes (except M53 where migration might take place, but the failure cause should still be high temperature since solder joint A was totally melted during stressing). I will focus on Type 3 failure in this dissertation since the primary concern in this research is migration of solder due to current stressing.

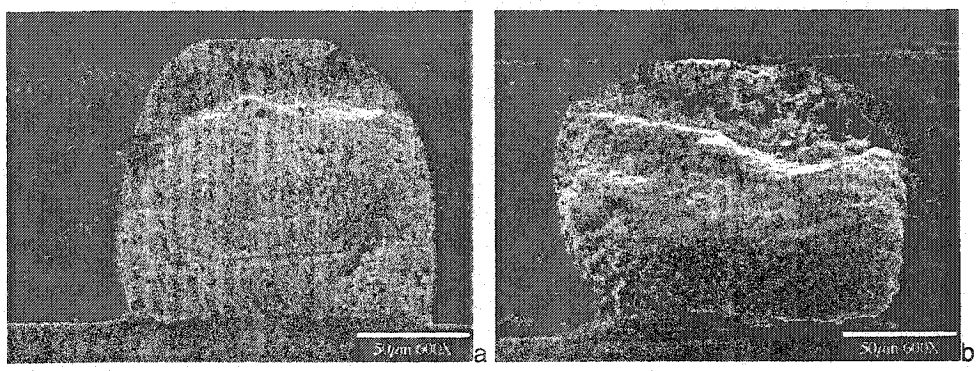


Figure 142 Secondary SEM (a) M34, solder joint A, 95 hours before failure (b) M42, solder joint A, 2 hours before failure

5.4.3 Void nucleation in solder joints during current stressing

To understand Type 3 failure due to electromigration and thermomigration, it is important to analyze the void nucleation modes in the solder joints during current stressing and their relationship with the failure of the test modules. Aside from the modules experiencing Type 3 failure, there were other modules in which we also observed void nucleation, but they did not fail, or failed due to mechanical re-polishing after indentation. We will discuss the void nucleation in all these modules. Four types of void nucleation modes were observed in these solder joints: 1) voids nucleate and grow on the Ni UBM-solder interface; 2) voids nucleate in the region near Ni UBM-solder interface; 3) Growth of pre-existing voids; 4) no void nucleation and growth after extensive stressing.

Table 11 Summary of void nucleation and growth modes in the experiments

Void nucleation and growth mode		
Mode 1 (on the UBM-solder interface)	M1 (solder A) M12 (solder A&B) M34 (solder B) M51 (solder A&B)	M6 (solder A&B) M14 (solder A&B) M42 (solder A&B) M53 (solder B)
Mode 2 (near the UBM-solder interface)	M34 (solder A) M56 (solder B)	M41 (solder B)
Mode 3 (growth of pre-existing voids)	M41 (solder A) M56 (solder A)	M52 (solder A&B)
Mode 4 (No void nucleation)	M7 (solder A&B) M15 (solder A&B)	M8 (solder A&B) M26 (solder A&B)

The voids were observed to nucleate and grow on the Ni UBM–solder interface (Mode 1) for the majority of the solder joints in our experiments, since this interface was the favorite site for void nucleation and growth. The combined electromigration and thermomigration effect leads to an atomic flux divergence in this region for both solder joint A and B (meaning the depletion of mass in the region). The direction of overall diffusion due to the combined effect of thermomigration and electromigration is from the Ni UBM–solder interface to the Cu plate in both solder joint A and B, as discussed in Section 5.3. Theoretical electromigration analysis indicates that the maximum tensile spherical stress will be generated in this region and the vacancy condensation will also occur in this region (Blech 1976;Blech and Herring 1976;Blech and Tai 1977;Blech and Kinsbron 1975;Kirchheim 1992;Korhonen et al. 1993;Park et al. 1999;Povirk 1997;Rzepka et al. 1997;Sarychev and Zhinikov 1999;Ye et al. 2003a). The driving force for void nucleation and growth is proportional to the tensile stress (Gleixner and Nix 1999). Gleixner and Nix (Gleixner and Nix 1996) numerically calculated the void nucleation rate in passivated interconnect lines due to electromigration and thermal stress based on the vacancy condensation theory (Raj and Ashby 1975;Hirth and Nix 1985). They suggested that void nucleation by vacancy condensation in the lattice is extremely low and would not be expected to happen in reality. Flinn (Flinn 1995) proposed the possibility that contaminants at the metal/passivation interface are acting as void nucleation sites in passivated metal lines. Gleixner and Nix (Gleixner and Nix 1996) analyzed the effect of contaminants on void nucleation and found that void formation at a flaw in the interface would require a considerably smaller stress than that in classical void nucleation theory. They further concluded that voids would grow only at the intersection

of the grain boundary with the passivation layer due to the large difference between the grain boundary and lattice diffusivities. For void growth to occur, atoms must be removed from the void surface and the grain boundary acts as an extremely fast path for material removal relative to the lattice (Gleixner and Nix 1996). Raj (Raj 1978) showed that heterogeneous nucleation at the triple junction of a second phase particle and a grain boundary was the most probable. Based on the above discussion, it is clear that the Ni UBM–solder interface is the naturally preferable site for void nucleation and growth. The voids would nucleate at the intersections of grain boundary in the Ni–solder intermetallic compound with the assistance of contaminants during manufacturing. This interface has the maximum atomic divergence which is favorable for void growth. Figure 143 and Figure 144 show examples of Mode 1 void nucleation and growth on the Ni UBM-solder joint interface.

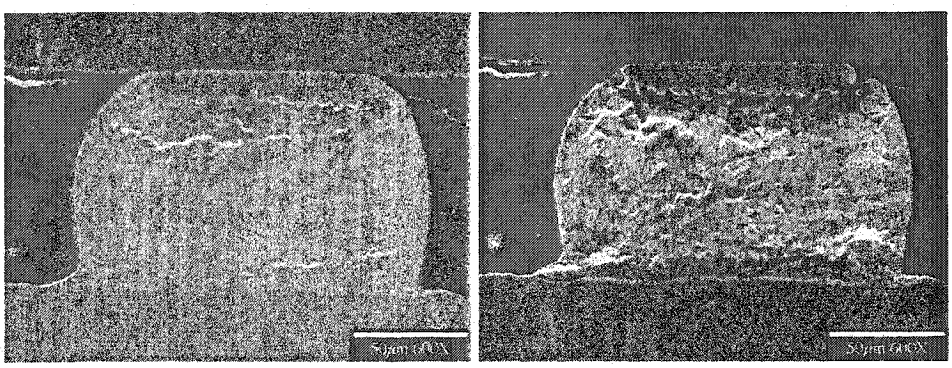


Figure 143 Secondary SEM of M12, solder joint A (L) 16 hours (R) 36 hours

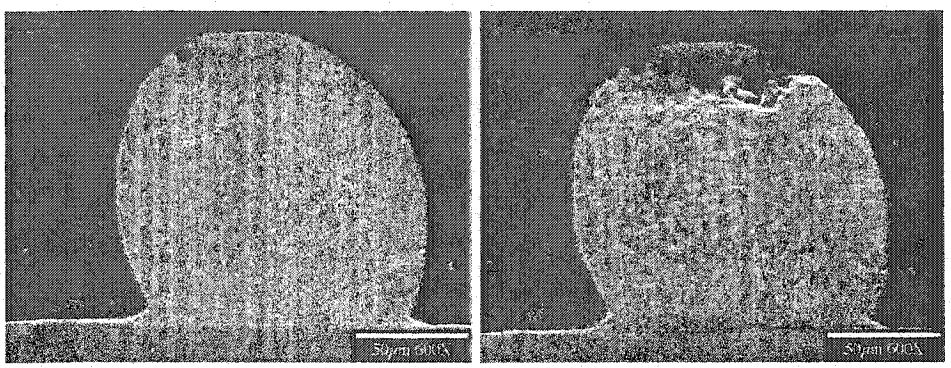
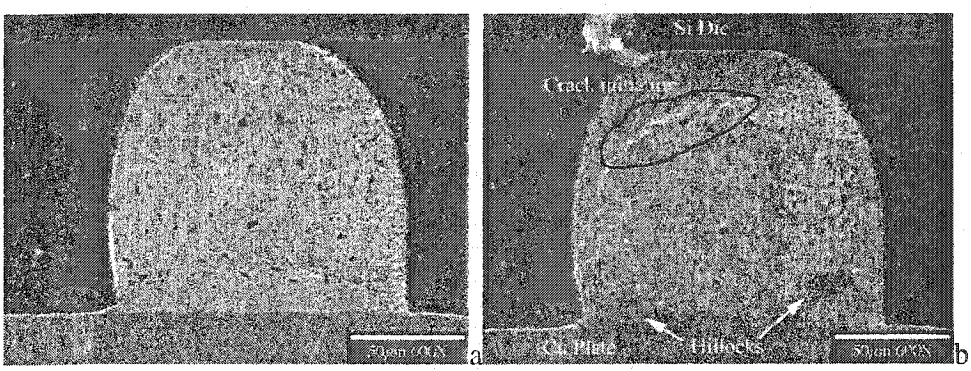


Figure 144 Secondary SEM of M42, solder joint A (L) 60.5 hours (R) 178 hours

Only three solder joints were observed to have Mode 2 void nucleation and growth. Figure 145(b) shows the void nucleation in the region near the Ni UBM–solder interface in M34, solder joint A after 268 hours of current stressing. Hillocks were observed to build up near the solder–Cu plate interface. Figure 145(c) shows that void growth and developing of severe depression in the region near the Ni UBM–solder interface after 444 hours of current stressing (note that the depression was filled with thermal compound left over when using thermal couple to measure the temperature). One unexpected observation is that new voids nucleated in the region of hillocks. The origin of these new voids is not clear. Since they were in the downwind region of thermomigration and electromigration, where atoms diffuse into and the material experienced compressive stress, the theory of void nucleation and growth under tensile spherical stress does not apply.



a b

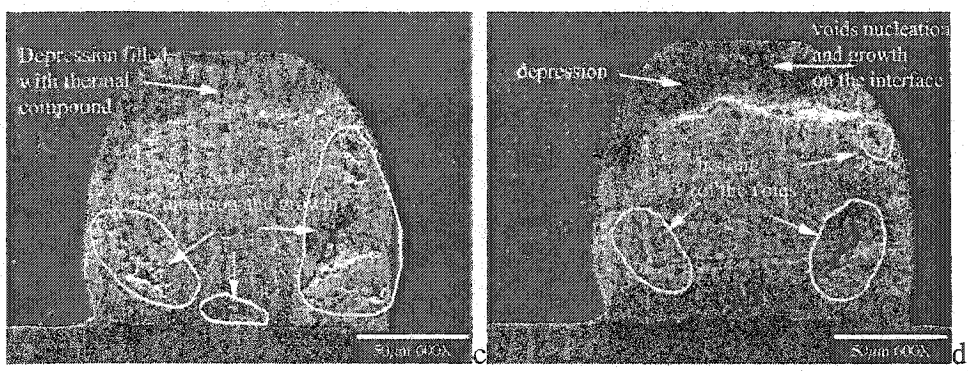


Figure 145 Secondary SEM of M34, solder joint A (a) 22 hours after re-polishing (b) 268 hours (c) 444 hours (d) 865 hours

One possible explanation of this observation is that the void nucleation and growth occur under shear stress. Xue et al. reported that the shear bands are the preferred sites for nucleation, growth, and coalescence of voids and, as such, are precursors to failure in titanium and Ti-6Al-4V alloy (Xue et al. 2002). In the hillocks region of solder joint A of M34, the material was subjected to biaxial compression stress according to the electromigration theory, but in the direction perpendicular to the solder surface the normal stress is zero. Therefore, in addition to the hydrostatic compression stress, the material in this region is also subjected to shear stress and this might be the cause of new void nucleation. Figure 145(d) shows the solder joint A after 865 hours of current stressing (which is 100 hours before final failure). More severe depression in the region of Ni UBM–solder interface was observed. Void nucleation on the UBM–solder interface was also found to initialize and grow, indicating that this site is still the preferred position for void nucleation even if the voids were initially nucleated elsewhere. An interesting observation in Figure 145 (d) is that the void nucleation in the hillocks regions was actually becoming smaller after the 400 more hours of current stressing since the previous SEM image. This probably indicates that after the voids in the hillocks region nucleated and grew to a certain extent, the stress that triggered void growth in this region

was released; therefore, no more growth of voids in this region was observed. Since the hillocks region is where the atoms diffuse into, the healing of the previous voids was observed instead. The void nucleation and growth in the hillocks regions does not seem to be the direct cause for the failure of the solder joint.

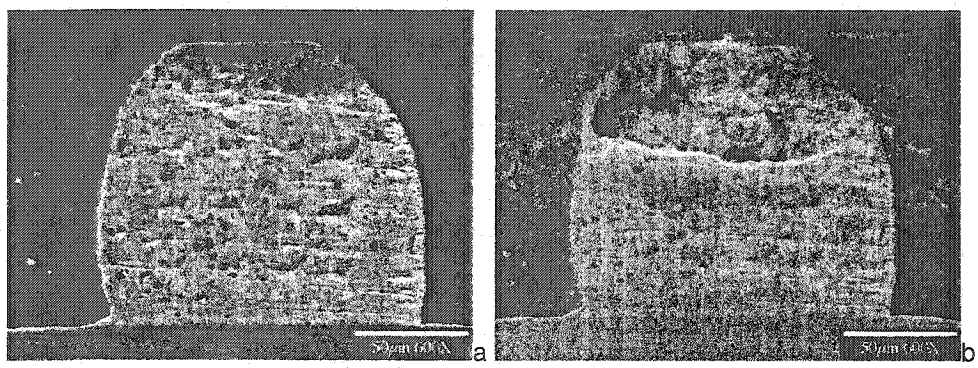


Figure 146 Secondary SEM of M34, solder joint A (a) 911 hours after re-polishing and indentaion (b) Failed after 960 hours

Figure 146 (a) shows the SEM image of solder joint A after re-polishing and nano-indentation testing. The hillocks were polished away and so were the voids in this region. However, the voids near the Ni UBM–solder interface still exist (note that the triangular depression on the surface of the solder joint were left over from nano-indentation). The SEM image after the failure indicates that the direct cause of failure was the severe void growth in the UBM–solder interface region, as shown in Figure 146(b). It is worth noting that M34, solder joint A was the only solder joint with void nucleation in the hillocks region among all the modules we tested. Void nucleation and growth in the region near the Ni UBM–solder interface was also observed in solder joint B of M41 and M56, but they were much less severe compared to solder joint A of M34 because the direction of thermomigration is opposite to that of electromigration in these solder joints. Of all the solder joints that were tested, only three solder joints had Mode 2

void nucleation and growth, indicating void nucleation in the region near UBM–solder interface is less favorable than that in the UBM–solder interface.

On the surface of some solder joints of the modules tested, there were pre-existing voids. These pre-existing voids may be produced during the reflowing process or created during polishing of the cross-sectioned surface. Some of these pre-existing voids led to Mode 3 void growth in which the growth of pre-existing voids causes the ultimate failure of the test module. According to our experimental results, whether or not these pre-existing voids grow depends on their locations; if the pre-existing voids are located in the region near the Ni UBM–solder interface, where atoms diffuse out due to the combined effects of thermomigration and electromigration, they are likely to grow. If the voids are not located in the UBM–solder interface region, they are very unlikely to grow. This observation is best presented in Figure 147. As shown in Figure 147 (a), there were several pre-existing voids on the cross-sectioned surface of solder joint A of M56. One small void with an irregular shape was located in the region near the UBM–solder interface. Several others were located near the Cu–solder interface, two of them with round shape et al. with an irregular shape. It is clearly shown in Figure 147 (b)-(d) that only the pre-existing void in the region near the UBM–solder interface grew dramatically to form a big crack in that area. On the other hand, other bigger voids near the Cu–solder interface did not grow very much, no matter what their initial shapes were, although they did change their shape a little bit possibly due to the local stress build up and local surface diffusion. This observation agrees with Lee et al.'s solder joint electromigration experiment (Lee et al. 2001a). Figure 147 (c) and (d) show that, besides severe void

growth in the region near the UBM–solder joint interface, two hillocks were gradually built up on the surface and a depression area was formed between these two hillocks.

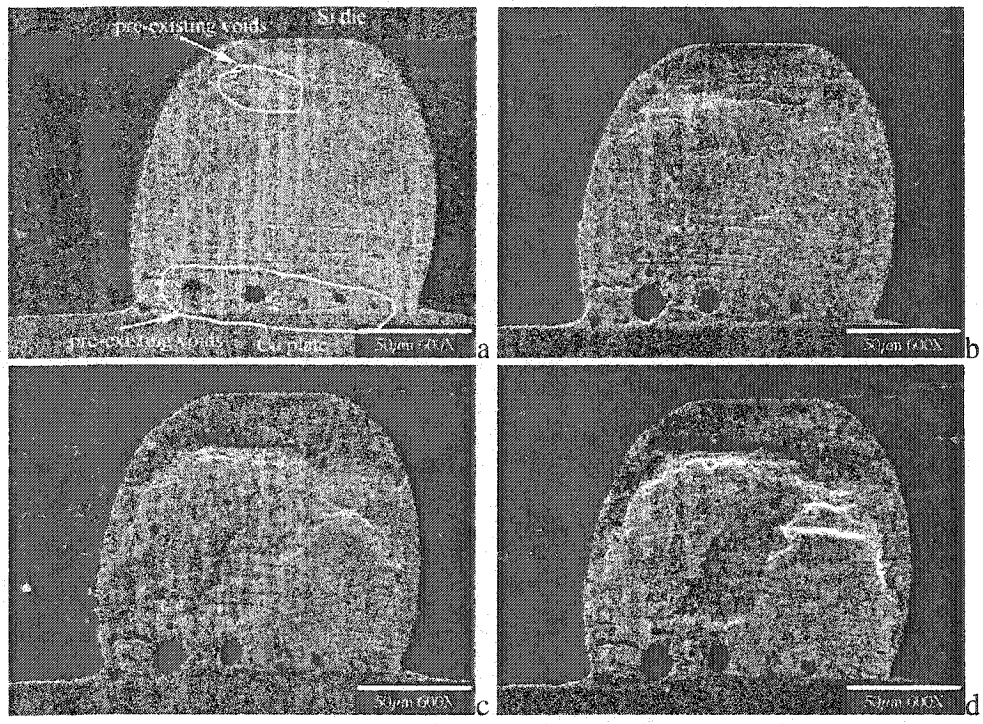


Figure 147 Secondary SEM of M56 solder A (a) initial (b) 269 hours after re-polishing (c) 932 hours (d) 1267 hours

This observation indicates that the diffusion process was not homogeneous within the solder joint. Careful examination of the phase structure reveals that the Pb rich phase in the depression region was not equiaxially shaped and had a preferred orientation compared to that in the hillocks regions, as shown in Figure 148. This preferred Pb phase orientation was formed during manufacturing and was preserved during current stressing. According to Kwok and Ho (Kwok and Ho 1988), the effective boundary diffusion coefficient, D_a, equals $\delta D_{gb}/d$, where δ is the grain boundary width, D_{gb} is the grain boundary diffusivity, and d is the average grain size. Although the Pb phase size is not the actual grain size, it is proportional to grain size for polycrystalline solids for diffusion purpose. The oriented eutectic structure indicates an oriented inequiaxed grain structure,

which leads to the difference of average grain size in different directions. This means the effective diffusivity may not be isotropic in this region, and therefore the diffusivity in the whole solder joint is inhomogeneous. The observation suggests that the microstructure of eutectic Sn/Pb solder joints affect its diffusion property and, therefore, the failure process under current stressing.

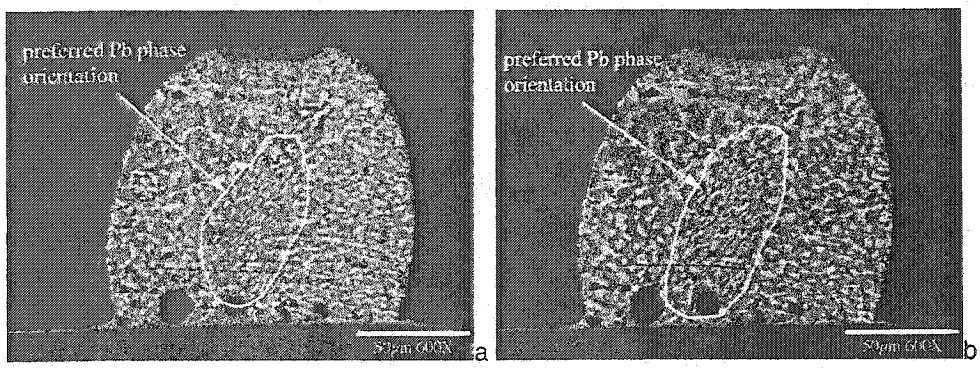


Figure 148 Backscatter SEM of M56 solder A (a) Initial (b) after 269 hours

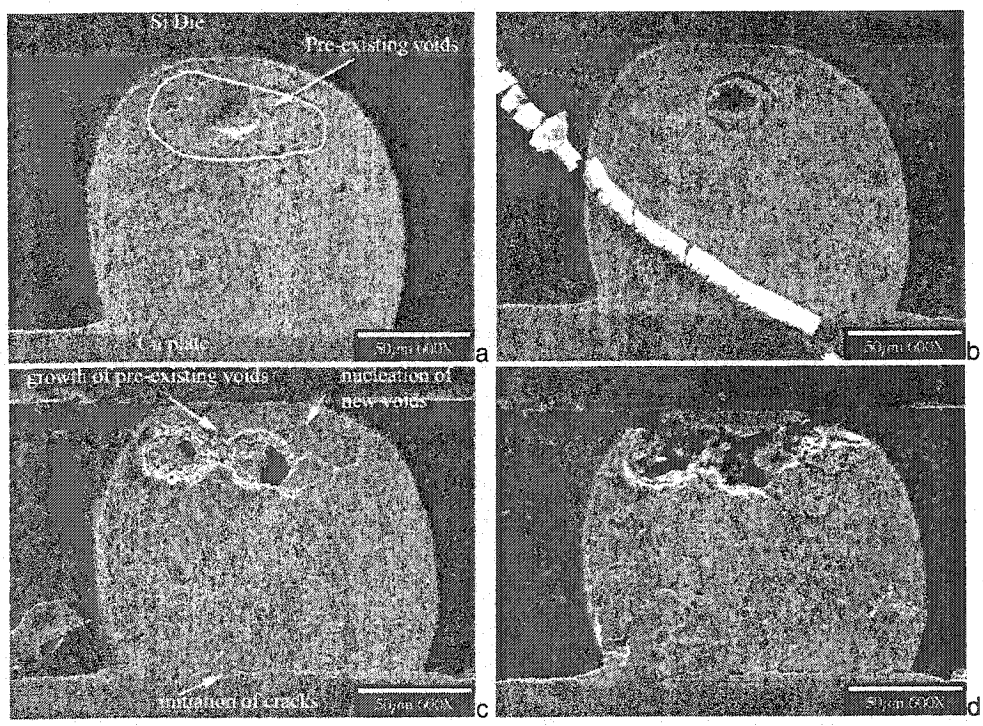


Figure 149 Secondary SEM of M41 solder A (a) initial (b) 37.5 hours after re-polishing (c) 60.5 hours (d) failure after 61 hours

Figure 149 shows another example of the growth of pre-existing voids. The pre-existing voids in solder joint A of M41 were located very near to the Ni UBM–solder interface and were produced during initial manufacturing. The pre-existing voids were observed to grow rapidly toward the UBM–solder interface and led to the ultimate failure of the module, as shown in Figure 149(d). New void nucleation on the UBM–solder interface was observed in addition to the growth of pre-existing voids during current stressing, as shown in Figure 149(c). Instead of observing hillocks building-up near the Cu–solder interface region, crack initiation was observed, as shown in Figure 149(c) and (d). The cracks finally interconnected to form a diagonal crack across the solder joint and a horizontal crack parallel to the Cu–solder interface. This observation reveals the complexity of the stress condition in solder joint during current stressing, although solder joint A of M41 was the only solder joint to observe this phenomenon.

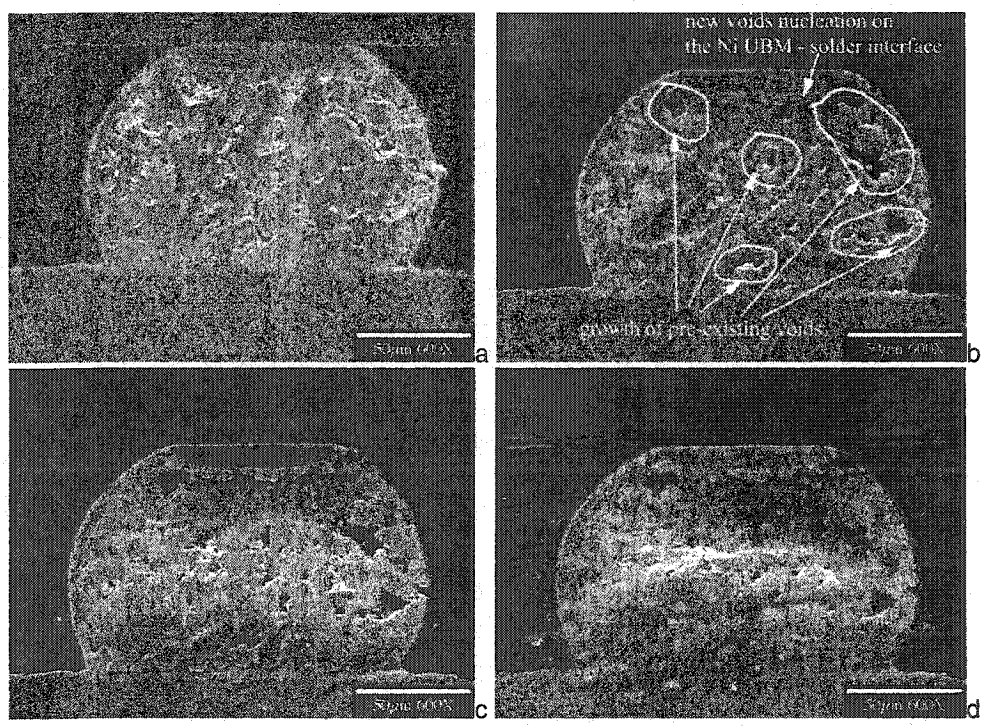


Figure 150 Secondary SEM of M52 solder A (a) initial (b) 66 hours (c) 590 hours (d) 914 hours

Different type of pre-existing multi-voids were observed in solder joints A and B of M52. All the pre-existing voids are distributed in the Pb rich phase, as shown in Figure 150(a). These voids were created during manufacturing and the reason for their formation only in the Pb rich phase is not clear. Some of the pre-existing voids were observed to grow after 66 hours of current stressing, as shown in Figure 150(b) and the growths of these pre-existing voids seemed to be restricted within the Pb rich phase. Some new void nucleation on the Ni UBM–solder interface was also observed, despite the existence of pre-existing voids. The pre-existing voids seemed to cease to grow after the voids occupied the whole area of former Pb phase. They would not expand into the Sn rich phase after certain amount of time of current stressing, as shown in Figure 150 (c) and (d). In the mean time, the newly nucleated voids on UBM – solder interface continued to grow. After 914 hours of current stressing, severe void growth and depression near the UBM–solder interface and hillocks build-up near solder – Cu interface were observed, as shown in Figure 150(d).

Some of the modules tested never experienced void nucleation and growth even after extensive current stressing, as shown in Table 11. M7 was subjected to low frequency PDC stressing at different current levels from 3A~7A with a duty factor of 0.96%. Although the peak current density in the solder joints were extremely high, the low duty factor prevented the void nucleation from being observed before the Al trace failed as explained in the previous section.

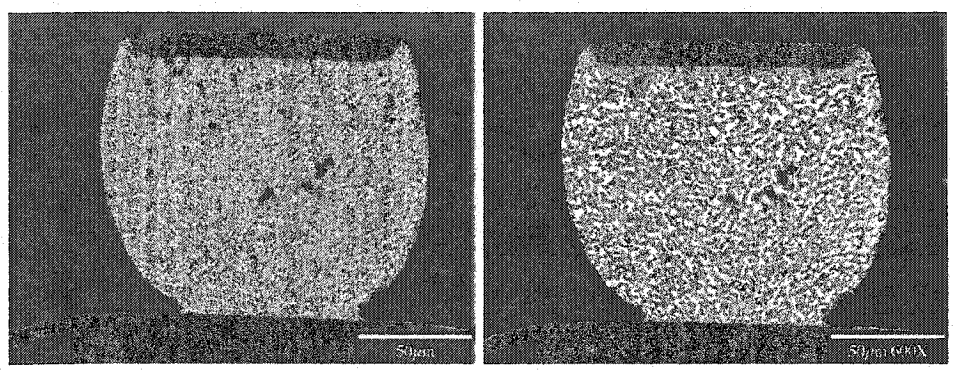


Figure 151 Backscatter SEM M8 solder A (L) initial (R) 149 hours

M8, M15, and M26 were all subjected to 0.5A of dc current stressing. Relatively low current level led to relatively low current density in the solder joints and less joule heating within the Al trace. Therefore, both the electromigration and thermomigration were less severe than solder joints in other modules where a higher level of current was applied. The calculated current density based on the estimated cross-section area in the solder joints of M8 and M26 range from 0.57 to $0.75\times10^4 A/cm^2$. Pb phase growth was clearly observed in the solder joints in both modules, such as is shown in Figure 151. Both modules were damaged due to the re-polishing after nano-indentation tests. The Pb phase coarsening within a relatively short period of time indicates that electromigration and thermomigration were operative in these solder joints during current stressing. The authors think that lower current density and lower stressing temperature lead to longer incubation time for void nucleation. Therefore, the voids in these solder joints did not have enough time to nucleate to an observable size before the modules failed due to mechanical polishing. On the other hand, when the current density and stressing temperature is very low, the effect of electromigration may become almost invisible even if the module is stressed for an extremely long period of time. This was the case in M15, where the estimated current density was $0.4\times10^4 A/cm^2$ and the stressing temperature was

only 40°C. Figure 152 shows only minimum microstructural change in solder joint A of M15 after an extensive 3000 hours of current stressing and no void nucleation was found. This indicates the possibility that there exists a threshold current density under which no electromigration failure occurs, such as the critical current density found by Blech (Blech and Herring 1976;Blech and Tai 1977) in his electromigration experiments of thin metal film under current stressing.

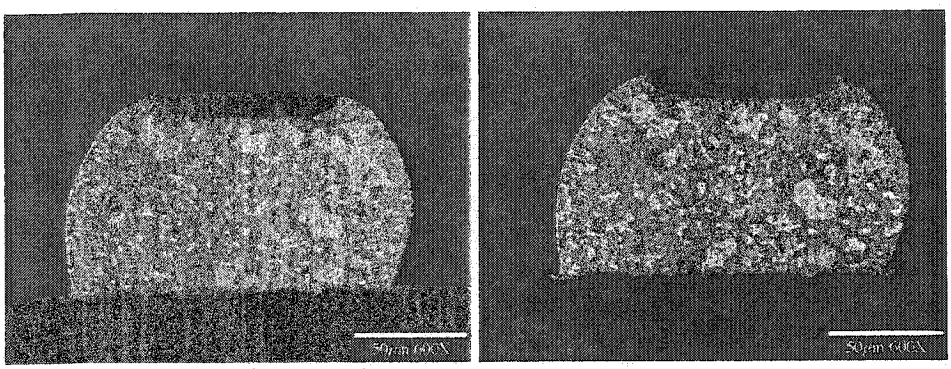


Figure 152 Backscattered SEM M15 solder A (L) 224 hours (after re-polishing) (R) 3156 hours

5.4.4 Discussions on Time to Failure

As discussed in the previous sections, only Type 3 failure, where void nucleation and growth were observed in solder joints during stressing, is caused by electromigration and thermomigration. Figure 153 shows the time to failure (TTF) versus current density in solder joint A of each test module since the degradation of solder joint A causes the eventual failure of the module as mentioned. The modules listed here were either subjected to electromigration and thermomigration failure (Type 3 failure) or such failure was imminent. It clearly shows that TTF decrease dramatically as current density increase but with two exceptions: M52 and M56, which are clearly not following this tendency and will be discussed later. The current density is not the only variable that

determines to TTF. Other variables, such as stressing temperature and temperature gradient, are also closely related.

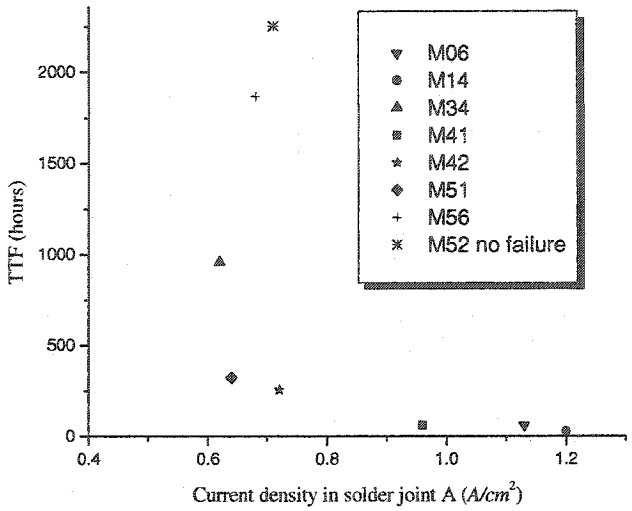


Figure 153 TTF vs. Current density

The most commonly used method for predicting the mean time to failure (MTTF) of metal interconnects for semiconductor devices subjected to electromigration failure is Black's law,

$$MTTF = \frac{A}{j^n} e^{Ea/kT} \tag{5.6}$$

where j is current density, n is the current density exponent which Black found to be 2, E_a is the activation energy of the failure process, k is Boltzman's constant, T is absolute temperature, and A is a constant (Black 1967;Black 1969). Since Black's law describes MTTF as only a function of temperature and current density, it cannot predict the variation in MTTF with the many other variables know to affect lifetime, as noted by Gleixner and Nix (Gleixner and Nix 1999). These include the microstructure of the interconnects, line dimensions and geometry of the particular alloy and compositions, and the condition of surrounding interfaces and boundary conditions (Attardo and Rosenberg 1970;Agarwala et al. 1972;Gleixner and Nix 1999;Korhonen et al. 1993;Lloyd

1999b;Blech 1976;Ye et al. 2003a). The n=2 behavior as proposed by Black is supported by many experimental and theoretical studies as the consequence of the counter diffusional spherical stress gradient generated during electromigration (Blech and Herring 1976;Korhonen et al. 1993;Kirchheim 1992;Clement and Thompson 1995). Besides its theoretical limitations, Black's equation is so simple and effective that it is still widely used. Black's equation was recently used in the failure analysis of solder joints under current stressing (Brandenburg and Yeh 1998;Lee et al. 2001a).

Table 12 TTF Regression based on Black's Law

M#	Current Density (10^4A/cm^2)	Temp. (K)	TTF Test (hours)	TTF predicted by regression (hours)	Regression Residual (hours)	Residual %	90.00% Confidence Limit	
6	1.13	413*	61	61.74	-0.74	-1.2	43.99	79.48
14	1.2	428*	26	33.13	-7.13	-27.4	20.34	45.91
34	0.62	373	960	953.98	6.022	0.6	872.22	1035.73
41	0.96	423	61	60.95	0.05	0.08	39.39	82.51
42	0.72	393	256	315.40	-59.40	-23.2	267.74	363.07
51	0.64	403	323	274.69	48.31	15.0	214.49	334.88
52**	0.71	383	>2254	480.65			435.96	525.34
56**	0.68	383	1868	524.0			460.55	587.45
15**	0.4	313	>4200	48033			16650	79417

Note: * temperature of this module is estimated
** module not used for regression

In this study, the TTF of solder joint under current stressing is compared to Black's law. A non-linear regression procedure is employed to determine the relationship between TTF and current density & temperature based on Black's law. The TTF data from the modules subjected to Type 3 failure are used for the regression process except M56 which is an exception as mentioned above. The current density exponent is assumed to be 2, as proposed by Black, since we do not have enough TTF data points to determine it ourselves. Because the measured stressing temperature on each module is changing during current stressing, an average value is used for the purpose of regression. In some modules, stressing temperature is estimated since no temperature was measured during

testing. The thermal gradient within the solder joint is not directly accounted for, but, as shown by coupled thermal electric FE simulation in the previous section, higher temperature on the die side indicates higher temperature gradients within the solder joint. The TTF data used for regression is listed in Table 12. Let $X = j$, $Y = T$, $Z = TTF$, $a = A$, $b = E_a / k$, the Black's equation to be fit is then $Z = \frac{a}{X^2}\exp(b/Y)$, where j is current density, T is absolute temperature, E_a is activation energy of failure process, and k is Boltzman's constant. The regression results are shown in Figure 154 and listed in Table 13.

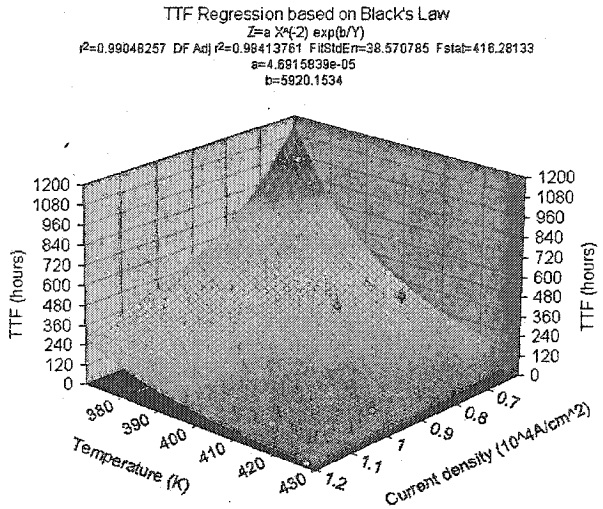


Figure 154 TTF vs. Current density & Temperature

Table 13 TTF regression results

Parmmeters	Value	Std Error	t-value	90.00% Confidence Limits		P>|t|
a	4.6916e-05	6.9821e-05	0.67195	-0.000102	0.000196	0.53843
b	5920.2	560.89	10.555	4724.4	7115.9	0.00046

The regression results of Black's equation from our experiment data is:

$$TTF = \frac{4.69\times10^{-5}}{j^2}\exp(5920.2/T) \qquad (5.7)$$

where TTF is in hours, j is in $10^4 A/cm^2$, and T is in $Kelvin$. The activation energy is calculated to be $b \times k = 5920.2 \times 8.62 \times 10^{-5} = 0.51 eV$, with a 90% confidence limit of 0.47~0.61eV. This activation energy is a little bit lower than the 0.8eV reported by Branderburg and Yeh (Brandenburg and Yeh 1998) from their MTTF experiments on flip-chip solder joints. They also found the current density exponent to be 1.8 instead of 2, as proposed by Black.

The TTF predicted by the regression is listed in Table 12 to compare it to the actual TTF in the experiments. This shows that the TTF predicted by the regression model does not match all the test results. The regression model predicts that the TTF for M15 is 48033 hours; this prediction is reasonable compared to our experimental observation where only slight microstructural change was observed on this module after over 4000 hours of current stressing. But TTFs of M52 and M56 clearly do not obey this regression model. In both cases the actual TTF is over 3 times longer than that predicted by the regression model. The authors think this observation is related to the void growth mode in these two modules. The failure mechanism of all the modules that match the regression model is that nucleated voids or pre-existing voids grow severely on the Ni UBM–solder interface, which leads to the ultimate failure. In the case of M52, the growth of pre-existing voids within the Pb rich phase in solder joint A clearly delayed the void growth on the UBM–solder interface, as shown in Figure 150. For M56, the growth of pre-existing voids in the region near the UBM–solder interface efficiently eliminated the void growth on the UBM–solder interface. As shown in Figure 147, the void growth on the UBM–solder interface in solder joint A was gentle even when very severe voids were forming in the region near the UBM–solder interface after 1267 hours of current stressing.

As mentioned above, the UBM–solder interface is the most favorable site for void nucleation and growth; therefore, the void nucleation and growth are the fastest at this site. The explanation for the TTF exceptions of M52 and M56 is simple: if the growth of pre-existing voids within the Pb rich phase of solder delays the void growth on the UBM–solder interface, the failure process will be delayed, as is the case in M52. If the major void growth is not on the UBM–solder interface, the void growth process is much slower and leads to a much longer TTF.

More importantly, Black's model does not include the effect of thermomigration on lifetimes of solder joints under current stressing. For instance, consider two solder joints which have the same average temperature due to joule heating under the same current density; however, the temperature is uniform in one solder joint and there is a 20°C temperature difference in another one as shown in Figure 155. Black's model would predict the same lifetime for both solder joints, which is not correct. As we already know, the thermal gradient in the second solder joint is high enough (2000°C/cm) to trigger thermomigration, which would significantly reduce the life time of the solder joint. This further indicates that the employment of Black's law on predicting the failure of flip-chip solder joints needs great scrutiny.

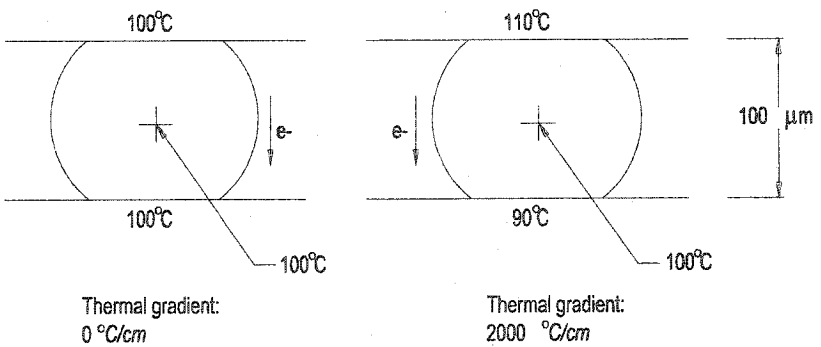


Figure 155 Solder joint with or without thermal gradient

5.4.5 Effects of Ni Barrier Layer on Copper Plate

As mentioned in Section 5.2, there are two different treatments of Cu plate surface: one with plated Ni barrier layer and one without. The Ni barrier layer provides a diffusion barrier between the solder joint and its copper substrate.

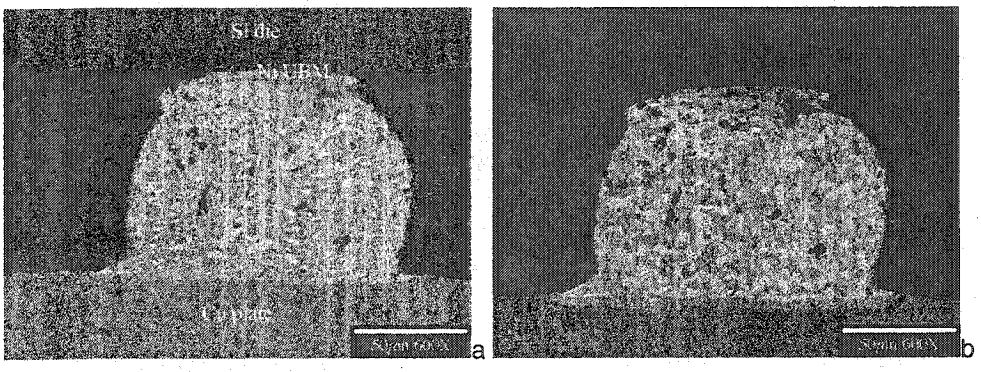


Figure 156 Backscatter SEM of M14, solder joint A (a) initial (b) after 16 hours of stressing

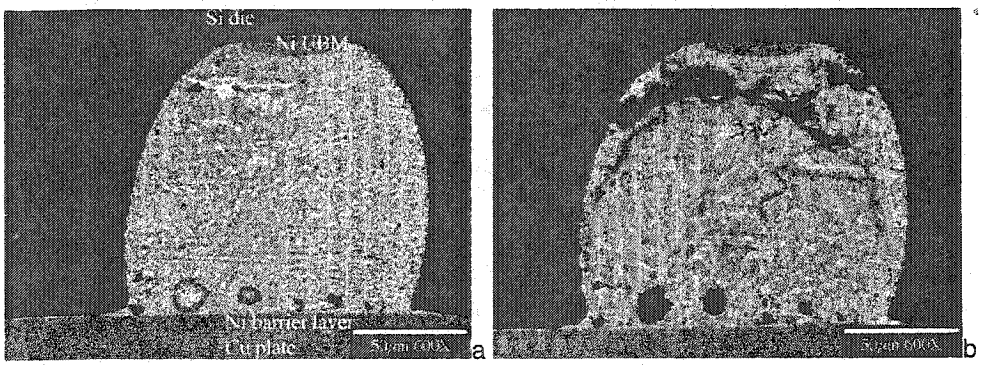


Figure 157 Backscatter SEM of M56, solder joint A (a) initial (b) after 1267 hours of stressing

Figure 156 shows that without the Ni barrier, the solder (mostly Tin) diffused into the Cu plate during current stressing. On the other hand, the Ni barrier totally blocked any solder from diffusing into its substrate, as shown in Figure 156. Other than this distinction, the authors did not find any evidence that the Ni barrier layer alters the failure process of solder joints under current stressing. Because the Ni barrier layer is located on the side into which atoms diffuse, and because of the combined the effects of electromigration and thermomigration, its existence would only affect the formation of

hillocks and the local stress state. The failure of the module is controlled by a mechanism of voids formation and growth, instead of hillocks growth. Therefore, the Ni barrier layer does not have a direct impact on the failure of the solder joints under current stressing.

5.4.5 Conclusion

The failure modes of flip-chip solder joints under current stressing were analyzed based on the experiments of 20 flip-chip modules. Three different failure modes were observed. Among them, only Mode 3 failure is caused by the combined effect of electromigration and thermomigration, where void nucleation and growth contribute to the ultimate failure of the module. The void nucleation and growth in a solder joint during current stressing is discussed in detail. The Ni UBM–solder interface is the favorite site for void nucleation and growth. The effect of pre-existing voids on the failure process of a solder joint is found to be dependent on their location. Black's equation is found not to be a reliable way to predict the lifetime of a solder joint under current stressing. This is because different void nucleation and growth mechanisms exist in the failure process of the solder joints and the fact that Black's equation cound not consider the effect of thermomigration on the lifetime of a solder joint.

5.5 Pb Phase Coarsening Under Electric Current Stressing

Coarsening of eutectic Pb/Sn flip-chip solder joint under current stressing is studied. Phase growth is observed under different current densities and stressing temperatures. Higher current density leads to faster coarsening. Based on the test results,

a grain coarsening equation including the influence of current density is proposed as, $d^n - d_0^n = Kj^m t$. The current density exponent m is found to be 3, and phase growth exponent n is 5.5. Within our test temperature range, electric current seems to have a greater influence on phase growth of the solder joint than does temperature or thermomigration caused by the temperature gradient due to Joule heating during current stressing.

5.5.1 Introduction

The reliability of solder joints under thermomechanical fatigue loading has been extensively studied in recent years (Solomon 1986;Solomon and Tolksdorf 1996;Chow and Wei 1999;Dasgupta and Hu 1992;Basaran and Tang 2001;Basaran and Chandaroy 1998). Morris, et al.(Morris Jr. et al. 1991) stated that the thermal fatigue of Pb/Sn eutectic solder can be characterized by microstructural coarsening or phase growth in the fatigue region. Frear, et al.(Frear et al. 1997) studied the microstructural evolution of the solder and suggested that phase size be a damage parameter to evaluate thermal fatigue lifetime.

Pb phase growth was observed in flip-chip solder joints under current stressing in our experiments. We expect that this coarsening is also related to the reliability of solder joints under current stressing in two ways: 1) stress builds up in the solder joint due to electromigration and thermomigration where phase coarsening affects its mechanical reliability; 2) grain coarsening changes the effective diffusivity of the solder joint which will alter the migration process. Many researchers proposed coarsening models for solder under thermomechanical loading, but the coarsening model for solder under current

stressing is still open for discussion due to the lack of experimental results. The understanding of the influence of an electric current on a metal alloy solid state transformation is still far from complete. Some examples of influence of an electric current include intermetallic compound formation, precipitation, recrystallization, and grain growth (Conrad 2000). The phase transformations mentioned here are all diffusion-controlled. Therefore electromigration is obviously expected to be important when considering the influence of an electric current.

Chen, et al. (Liu et al. 1998;Chen et al. 1998) found out that, in many diffusion couples, electric current affected the thickness of the intermetallic compound layers that normally form without a current. They found that their experiment results on the diffusion couples were in qualitative accord with electromigration. Xu et al.(Xu et al. 1988) reported that a continuous DC current of ~$10^3 A/cm^2$ enhanced the recrystallization rate of cold worked α-Ti and gave a finer recrystallized grain size. At higher annealing temperatures, the current enhanced grain growth, and the degree of coarsening increases with current density. Maurer and Gleiter (Maurer and Gleiter 1985) have shown that conduction electrons have an influence on the structure and energy of a grain boundary. Koppenaal and Simcoe (Koppenaal and Simcoe 1963) reported that a dc current of ~$10^3 A/cm^2$ enhanced the precipitation rate of an Al-4wt.%Cu alloy as determined by resistivity measurements. The precipitation rate increases in an approximately linear fashion with current density beyond a critical value of ~$10^3 A/cm^2$. Electric current was also found by researchers (Teng et al. 1996;Lai et al. 1995;Lai et al. 1989) to accelerate the crystallization of rapidly-quenched amorphous alloys (Fe-Si-B). However, until today our understanding of the detailed atomic mechanisms pertaining to the effects of a current

on phase transformation is still very rudimentary(Conrad 2000). This section reports the Pb phase growth in flip-chip solder joints with different initial phase size, different current density and different stressing temperature. The results are compared to the existing phase coarsening models.

5.5.2 Experimental

As described in Section 5.2, the test modules were taken off circuit for SEM analysis during the course of testing. The Pb phase size of solder joints was measured along the course of current stressing following ASTM standard E1382(1999a). According to ASTM standard E1382, several methods can be used to determine average grain size: grain intercept lengths, intercept counts, intersection counts, grain boundary length, or grain areas. The individual grain area method for a two-phase structure is used in this experiment, since digital imaging processing software is employed. The area of each Pb phase interior, A_i, on the solder surface is measured for every Pb phase region. The average phase region area, $\overline{A}_{Pb}$, is determined by:

$$\overline{A}_{Pb} = \frac{\sum_{i=1}^{N} A_i}{N_{Pb}} \qquad (5.8)$$

where N_{Pb} is the total number of Pb phase regions on the solder surface. The average Pb phase region area was measured for each solder joint before and after certain hours of current stressing at room temperature. The average phase area was measured directly on the SEM backscattered images of cross-sectioned solder joint. The area fractions of Pb phase region for initial as-reflowed solder joints, $N_{Pb}\overline{A}_{Pb} / A_{Total}$, are measured between 26.5%~29.1% and are in accordance with predicted volume fraction of Pb Phase from

phase-diagram (Jung and Conrad 2001a). Digital image processing software *Image Pro Plus*® (2000) was used to automatically identify the phase region boundary, and measure phase area and average diameter. On the SEM backscatter image, the light region corresponds to the Pb rich region, and the dark region corresponds to the Sn rich region, because of their difference in elemental numbers. By setting the gray scale limits in *Image Pro Plus*®, the Pb rich region boundary can be detected, and average area data measured. The Pb phase region is outlined by the software in Figure 158.

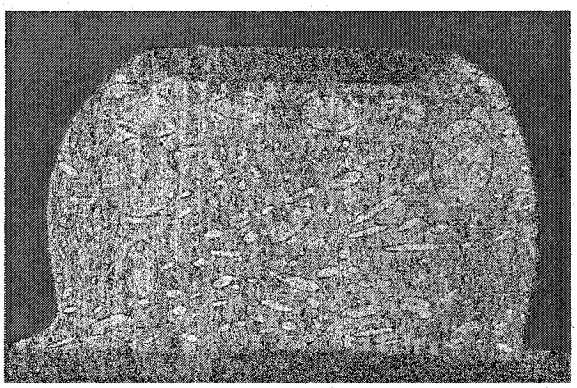
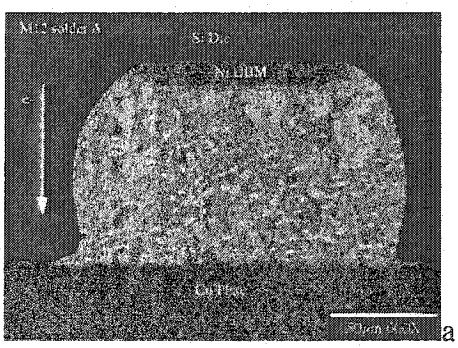


Figure 158 Pb phase outlined by ImagePro plus

During the course of current stressing, the average Pb phase size was observed to grow. Voids were observed to nucleate near the cathode side and hillocks observed near the anode side. Figure 159 shows the SEM backscattered image of solder A from module #12 during current stressing, where phase coarsening is clearly shown. Intermetallic compound growth is also clear on the solder/Cu plate interface.



a

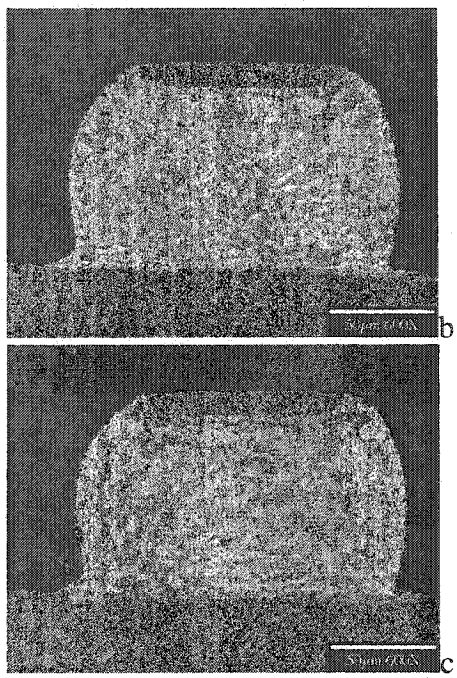


Figure 159 SEM backscatted image of solder joint A from module #12: a)initial b)16 hours c)36 hours

5.5.3 Test Results

Pb phase growth as observed in 14 Pb/Sn eutectic flip-chip solder joints under different current densities from 0.4×10^4 to 1.13×10^4 A/cm^2 is reported in this section. In order to compare the phase size growth between different solder joints, the normalized phase size is defined and used. Since we measure the average area of the Pb phase, phase size is defined as the square root of average phase area, $d=\sqrt{\bar{A}_{Pb}}$. Normalized phase size is further defined as phase size divided by the initial phase size for each solder joint, or d/d_0, where d_0 is the initial phase size. The initial Pb phase size is measured from microstructure of solder joint before stressing at room temperature. Thus, every solder joint has an initial normalized phase size of 1. Since the actual Pb rich phase is a three dimensional microstructure, the measured two dimensional phase size on the polished surface is dependent on the position of polishing. A re-polishing will thus undoubtedly

alter the measured phase size even without any current stressing. The phase size reported in this section does not include any data measured after re-polishing. If a module is re-polished at a very early stage of current stressing, the initial phase size is taken as the measured phase size right after that re-polishing, but no data is collected after further re-polishing. The solder joints reported in this section are named as M##A or M##B, where M## indicates the module number. Letter A or B indicates if it is solder joint A or solder joint B, as in Section 5.2. Thus, M8A represent solder joint A on module #8. Figure 160 shows the normalized phase size d/d_0 vs. current stressing for all the 14 solder joints. All solder joints experienced phase growth except M15A and M15B, which have the lowest current density (0.4×10^4 A/cm^2) and temperature (40ºC) in the group. The current density, temperature, and initial phase size of each solder joint are listed in Table 15 in the following section. The curves in Figure 160 look scattered because of the different current density in each solder joint.

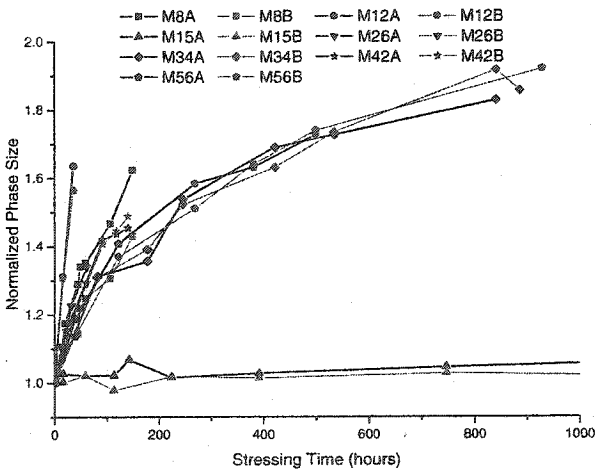


Figure 160 Normalized Phase Size vs. Stressing time

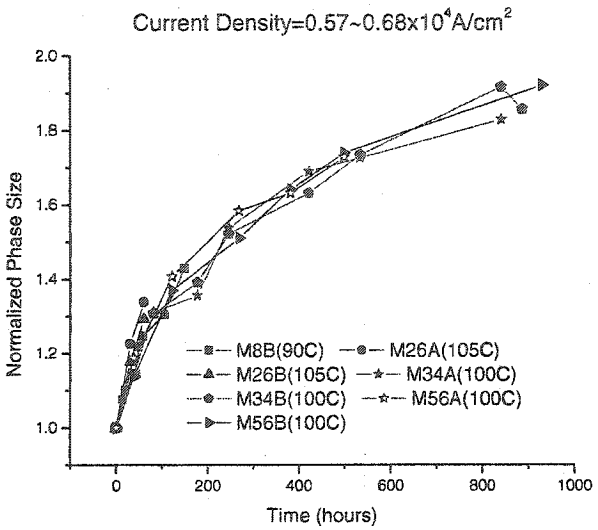


Figure 161 Normalized phase size vs. stressing time of solder joints with current density between $0.57 \sim 0.68 \times 10^4\ A/cm^2$

Figure 161 shows the normalized phase size vs. stressing time for solder joints with a current density between $0.57 \sim 0.68 \times 10^4\ A/cm^2$ only. The number in the parenthesis in the legend area shows the stressing temperature for each module which is the temperature measured on the silicon die. It shows that M26A and M26B, with a slightly higher stressing temperature of 105°C, have a slightly more rapid growth rate than the rest of the solder joints, but it is well within the experimental error range. Figure 162 shows the normalized phase size vs. stressing time for solders with different current density from $0.4 \sim 1.13 \times 10^4\ A/cm^2$. The stressing temperatures of these solder joints were between 90~120°C, except M12A (no temperature measured) and M15B (40°C). This observation shows very clearly that higher current density leads to more rapid phase coarsening. It is our understanding that, within the temperature range we tested the specimens, current density seems to be a more prominent factor to the Pb phase

coarsening than temperature, although temperature certainly has effect on this process because of the Arrhenius relationship between diffusivity and temperature.

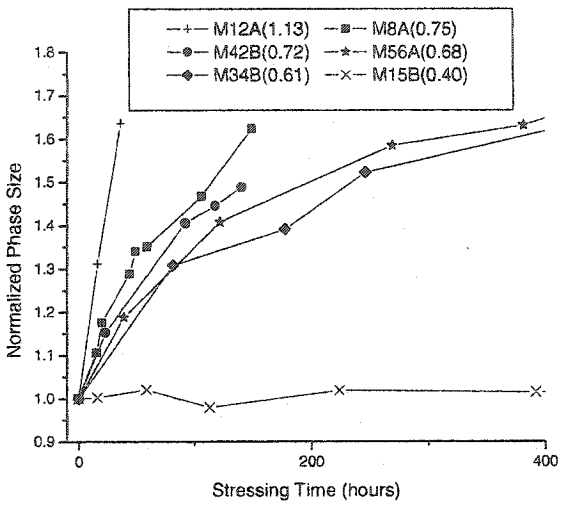


Figure 162 Normalized phase size vs. stressing time of solder joints with current density between $0.4 \sim 1.13\times10^{4}\,A/cm^{2}$

5.5.4 Discussions

For over a century, researchers have observed, analyzed, and attempted to model the microstructural evolution of polycrystalline materials. Understanding microstructure is critical because it governs the mechanical, thermal, and electrical properties of engineered materials. Burke and Turnbull (Burke and Turnbull 1952) proposed the conventional grain growth law for polycrystalline materials as:

$$\dot{d} = \frac{K}{d^{n-1}}, \tag{5.9}$$

where d is grain size, $\dot{d}$ is the grain size growth rate, K is the grain boundary mobility parameters, and n is an exponential constant, empirically between 1.5 to 9(Ng and Ngan 2002;Chen and Spaepen 1991). Burke and Turnbull further proposed that the parameter K has an Arrhenius form, $K = K_0 e^{-Q/kT}$, where K_0 is a constant, Q is the grain growth

activation energy, k is the Boltzman's constant, and T is absolute temperature. Integrating Burke and Turnbull's grain growth equation gives:

$$d^n - d_0^n = Kt\,, \tag{5.10}$$

where d_0 is the initial grain size at the test temperature. Researchers since then elaborated this grain growth law for different applications. For example, Hacke et al.(Hacke et al. 1993) proposed a cubic Pb phase coarsening model for eutectic Pb/Sn solder alloy under thermal mechanical fatigue loading:

$$d^3 - d_0^3 = \frac{ct}{T} e^{-Q/kT}\,, \tag{5.11}$$

where c is a kinetic factor that depends on matrix composition, and Q is the activation energy for volume diffusion. Subsequent work by Jung and Conrad gave n=4.1±0.15 and Q=39.8k*J/mole*, which is for grain boundary diffusion (Jung and Conrad 2001b). Upadhyayula (Upadhyayula 1999) modified this model to include the mechanical stress influence as:

$$d^3 - d_0^3 = \frac{ct}{T} e^{-q/kT} (1 + (\frac{\Delta\tau}{c_2})^{n_c}) \tag{5.12}$$

where $\Delta\tau$ is the stress range, n_c is the stress exponent, and c_2 is the reference stress.

Unfortunately, these coarsening models cannot be directly used in modeling the phase growth of eutectic solder alloy under current stressing, since none of them included the influence of electric current. Based on experimental results shown in Figures 160-162, the phase growth of the individual solder joint seems to obey Burke and Turnbull's exponential growth law. This is verified by re-plotting phase size vs. time on a log-log scale as shown in Figure 163. This clearly shows that phase size vs. time curves now

become close to straight lines in log scale, indicating the powered relationship between phase size and time.

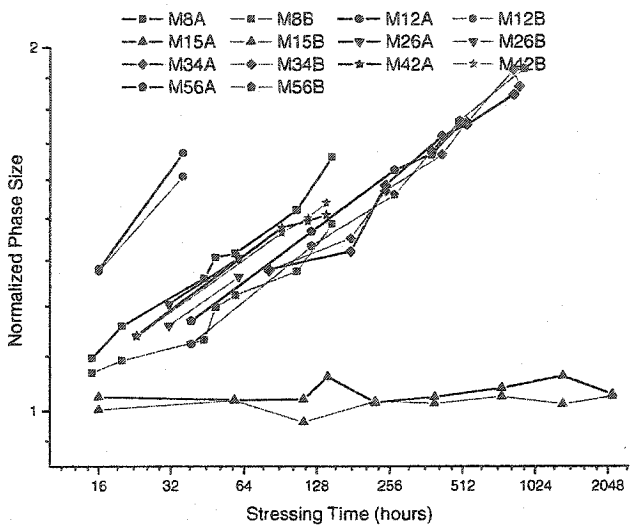


Figure 163 Log-log plot of Normalized Phase Size vs. Stressing time

Nonlinear regression procedure is used to determine the exponential n in Burke's coarsening law for each solder joint from the experiment results. The Burke's grain growth equation is rewritten as

$$(\frac{d}{d_0})^n = 1 + \frac{Kt}{d_0^n} \tag{5.13}$$

thus

$$\frac{d}{d_0} = (1 + \frac{Kt}{d_0^n})^{\frac{1}{n}}. \tag{5.14}$$

where d/d_0 is the normalized phase size used in the experiment. Let $Y = d/d_0$, $X = t$, $B_1 = K/d_0^n$, and $B_2 = n$. We are now using the experimental data of each solder joint to fit equation $Y = (1 + B_1 X)^{\frac{1}{B_2}}$. Table 14 gives the regression results for solder joint M56B. The value of exponent n for solder joint M56B is about 5. The 90% confidence range is from 4.42 to 5.64. Figure 164 shows the comparison between the test data and fitted curve.

Table 14 Regression result for solder joint M56B

Variable	Value	Standard Error	t-ratio	Prob(t)	90.00% Confidence Limits	
B_1	0.02848	0.00489	5.81611	0.00212	0.01862	0.03835
B_2	5.03381	0.30218	16.65840	0.00001	4.42492	5.64270

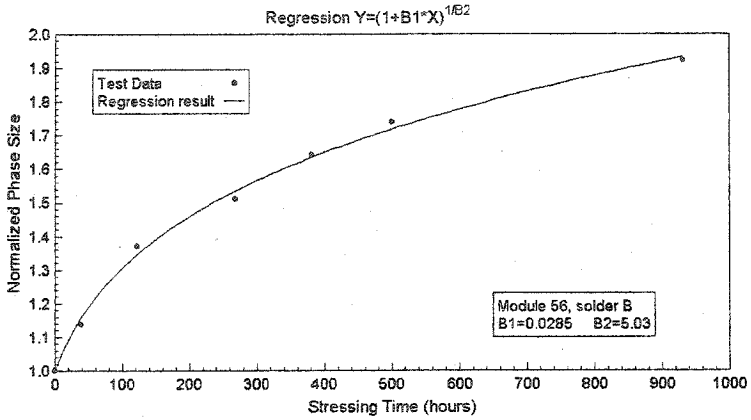


Figure 164 Nonlinear regression for solder joint M56B

The same nonlinear regression procedure was applied on each solder joint and the results are summarized in Table 15 along with the information of current density, temperature, initial phase size for each solder joint. We should mention that for solder joints M12A, M12B, M26A, and M26B, there are only 3 data points available for each solder joint in the nonlinear regression procedure, which is insufficient for this highly nonlinear regression. For the rest of the solder joints, the phase growth exponent ranges from 4.4 to 6.2. These values are much higher than 3 as proposed in Hacke's (Hacke et al. 1993) eutectic solder coarsening model and a value of 4 of later work by Jung and Conrad (Jung and Conrad 2001b). In the earlier section, we mentioned that the possible thermomigration may have the same or opposite direction with electromigration in solder joint A or solder joint B, respectively. But as shown in Table 15, there is no big difference in the phase growth exponent n between solder A and solder B for each test module. If the current densities in both solder joints in a single module is close to each other, their phase size vs. time curves also appear close to each other. These observations

suggest that in our experiments the influence of electric current on phase coarsening is much greater than the possible influence of the thermomigration due to Joule heating during current stressing.

Table 15 Regression results for $Y = (1 + B_1 X)^{1/B_2}$

Module#	Current density ($10^4 A/cm^2$)	Temperature ($^\circ C$)	Initial phase size (μm)	$B_1 = K / d_0^n$	$B_2 = n$
M8A	0.75	90	1.88	0.0473	4.41
M8B	0.57	90	1.97	0.0253	4.50
M12A	1.13	n/a	2.66	0.0385	1.77
M12B	0.88	n/a	2.40	0.0704	2.82
M15A	0.40	40	2.8	n/a	n/a
M15B	0.40	40	3.14	n/a	n/a
M26A	0.57	105	2.16	0.0694	5.67
M26B	0.57	105	1.81	0.0282	3.90
M34A	0.62	100	2.32	0.0392	5.73
M34B	0.61	100	2.12	0.0323	5.33
M42A	0.72	120	2.71	0.0719	6.20
M42B	0.73	120	2.52	0.0501	5.20
*M56A	0.68	100	1.88	0.0549	6.14
*M56B	0.64	100	2.06	0.0285	5.03

Note: * Temperature listed for M56 is the average for the first 800 hours of stressing, which is different from the average temperature for the whole stressing period as used in Section 5.4 for TTF estimation.

Since the Pb phase growth of solder joints under current stressing is closely related to the current density, as clearly shown in Figure 162, we propose a phase growth evolution that includes the influence of electric current by adding a current density term to Burke's grain growth equation:

$$d^n - d_0^n = K j^m t, \tag{5.15}$$

where j is the current density, and m is the current density exponent. The normalized form is:

$$\frac{d}{d_0} = (1 + \frac{K}{d_0^n} j^m t)^{\frac{1}{n}} \tag{5.16}$$

Let $Z = d/d_0$, $X = t$, $Y = j$, $B_1 = K/d_0^n$, $B_2 = n$, and $B_3 = m$. We are now using the experimental data of all the solder joints to fit a single equation $Z = (1 + B_1 XY^{B_3})^{1/B_2}$, which involves two independent variables X (time) and Y (current density). The regression result is shown in Table 16. The exponent n is found to be about 5.5, and current density exponent m is about 3. The phase growth exponent n calculated in this model, 5.5, is close to the growth exponent calculated in Burke's grain growth model without current, 4.4~6.2. The comparison between the fitted surface and test data is shown in Figure 165.

Table 16 Nonlinear regression results with two independent variables

Parameters	Value	Std Error	t-value	90.00% Confidence Limits		P>|t|
B_1	0.14987989	0.030990236	4.836358518	0.098211774	0.201548005	0.00001
B_2=n	5.510654291	0.440952065	12.49717312	4.77548201	6.245826572	0.00000
B_3=m	3.065412008	0.244324285	12.54648921	2.658065141	3.472758875	0.00000

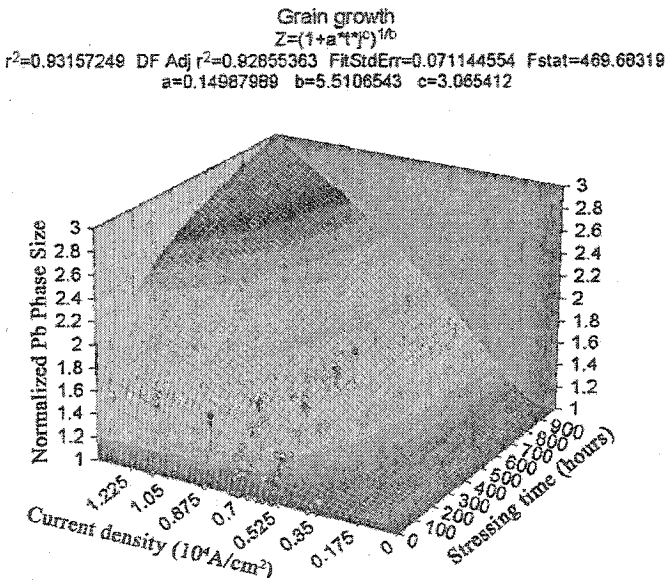


Figure 165 Regression of grain growth including the influence of current density

5.5.6 Conclusions

Experimental research on the Pb phase coarsening of eutectic Pb/Sn flip-chip solder joints under current stressing is reported. Pb Phase growth is observed under different current density and temperature. Higher current density leads to faster Pb phase coarsening. Based on the test results, a Pb phase coarsening model that includes the influence of current density is proposed: $d^n - d_0^n = Kj^m t$. The current density exponent m is found to be 3, and the phase growth exponent n is found to be 5.5. Electric current seems to have a bigger influence on phase growth in solder joints than temperature or thermomigration caused by the temperature gradient due to joule heating during current stressing in our test temperature range. In order words, for the temperature range we have used, the influence of current density was much more significant than that of temperature.

5.6 Mechanical degradation of solder joints under current stressing

Understanding the mechanical degradation of solder joints under high electric current stressing is an important step in developing a damage mechanics model to predict the reliability of solder joints. In this section, the experimental results of flip-chip solder joints under high current stressing are reported. Nano-indentation test data suggest that mechanical properties, such as elastic modulus, degrade in the localized area where voids nucleate during current stressing. Basaran and Tang (Basaran and Tang 2003) have shown that elastic modulus degradation is the most reliable and consistent parameter as a damage metric. The experimental results also show that the thermomigration due to the thermal gradient within the solder joint affects the mechanical degradation of solder joint during electric current stressing.

5.6.1 Instrumented Indentation Technique

Instrumented indentation testing (IIT) with a Nano-indenter is a powerful mechanical testing technique that can be used to test extremely small samples. Known as depth-sensing indentation, it collects the indentation load-displacement data precisely on a very small scale. Based on these data, it can measure the material properties such as hardness, Young's Modulus, and creep properties on very small (micron) scale specimens. Nano-indentation is very helpful for measuring mechanical properties on solder joints because of the size effect on material properties. By testing a specimen the same size as the actual system itself, the size effect is included. Bonda and Noyan (Bonda and Noyan 1996) have shown very effectively that at small scales material properties can be significantly different from those of bulk material. Figure 166 schematically shows the equipment for performing instrumented indentation tests, which consists of three basic components: (1) an indenter of specific geometry usually mounted to a rigid column through which the force is transmitted, (2) an actuator for applying the force, (3) a sensor for measuring the indenter displacement.

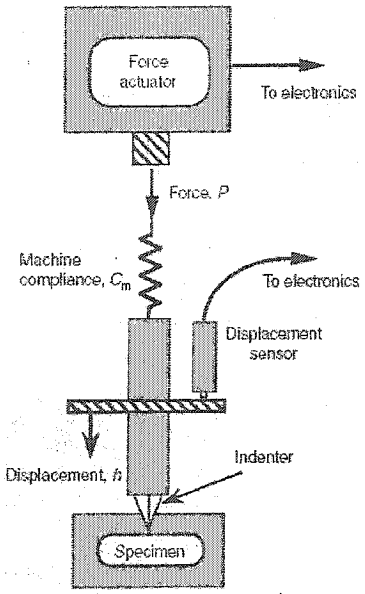


Figure 166 Schematic representation of the basic components of an IIT system (after Hay and Pharr (Hay and Pharr 2000))

The Continuous Stiffness Measurement technique (CSM), also known as Dynamic Stiffness Measurement, allows for the continuous measurement of elastic stiffness of contact, S, as the indenter is driven downward during loading. The measurement is accomplished by superimposing a small force oscillation on the primary loading signal and analyzing the resulting response of the system by means of a frequency-specific amplifier (Hay and Pharr 2000;Hay and Pharr 2000). With a continuous measurement of S, one obtains hardness and Young's modulus as a continuous function of depth of surface penetration. In the MTS Nano indenter XP unit with CSM system, intrinsic or reduced elastic modulus can be determined by the following relation (Hay and Pharr 2000):

$$E_r = \frac{\sqrt{\pi}}{2\beta}\frac{S}{\sqrt{A}} \tag{5.17}$$

where S is the elastic stiffness of contact (measured by CSM technique), A is the projected contact area, and β is a constant dependent on the geometry of the indenter. For

the MTS Nano-Indenter XP which uses a Berkovich tip, β=1.012. The Berkovich indenter tip has a three-sided pyramid shape. It has a centerline-to-face angle α of 65.3°, a projected area of 24.56 d^2 (d is the indentation depth), and a volume depth relation of 8.1873 d^3. Figure 167 shows a picture of the impression on an actual solder joint after indentation with Berkovich indenter.

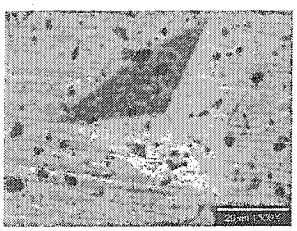


Figure 167 Indentation on a solder joint with a Berkovich indenter

The reduced modulus E_r is used to account for the fact that elastic displacement occurs in both the indenter and sample. The Young's modulus of the tested material, E, is calculated by:

$$\frac{1}{E_r}=\frac{1-\nu^2}{E}+\frac{1-\nu_i{}^2}{E_i} \tag{5.18}$$

where ν is the Poisson's ratio for the tested material, and E_i and ν_i are the elastic modulus and Poisson's ratio of the indenter, respectively. For diamond indenter, the elastic constants $E_i=1141GPa$ and $\nu_i=0.07$ are often used (Oliver and Pharr 1992;Simmons and Wang 1971). As noted by Hay (Hay and Pharr 2000;Hay and Pharr 2000), while it may seem counterintuitive that one must know the Poisson's ratio of the material in order to compute its modulus, even a rough estimate, say $\nu=0.25\pm0.1$, produces only about a 5% uncertainty in the calculated value of Young's modulus for most materials.

For the purpose of calculating E, the projected contact area, A, must be accurately obtained. The projected contact area is calculated by evaluating an empirically determined area function at the contact depth, h_c,

$$A = f(h_c) \tag{5.19}$$

This area function, also known as the shape function or tip function, relates the cross-sectional area of the indenter to the distance from its tip. Contact depth, h_c, is the depth over which the test material makes contact with the indenter, and is generally different from the total penetration depth, h, by

$$h_c = h - \varepsilon P / S\,, \tag{5.20}$$

where ε is a constant that depends on indenter geometry. The empirical value of ε for Berkovich indenter is 0.75(Oliver and Pharr 1992). P is the load applied to the test surface. This relationship is based on elastic contact theory, but it works well even when contact causes significant plastic deformation(Oliver and Pharr 1992). Figure 168 gives a schematic of the indentation process for an axisymmetric indenter, where h_c and h are shown schematically.

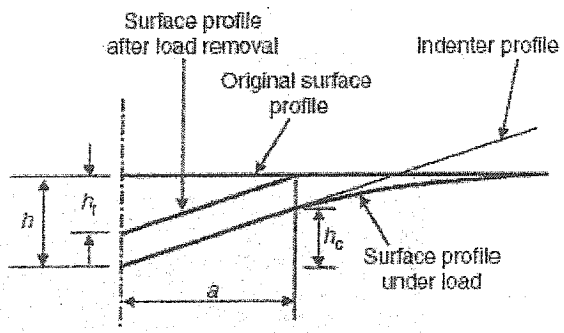


Figure 168 Schematic representation of a section through an axisymmetric indentation showing various quantities used in analysis [courtesy to Hay and Pharr (Hay & Pharr 2000)]

Once the projected contact area (A) and contact stiffness (S) are known, the Young's modulus can be calculated. In the experiment, indentation tests were conducted

on several locations on each solder joint in order to get the distribution of Young's modulus over the solder joint.

5.6.2 Preliminary Nano-indentation Testing

In the preliminary nano-indentation experiment, Modules #1, #2, and #3 were tested. Only Module #1 was subjected to current stressing. In order to measure the change in mechanical properties of solder joints before and after current stressing, test Modules #2 and #3 were tested to provide initial mechanical properties of the solder joints before current stressing. To perform the nano-indentation test on the solder joint, the test modules was cross-sectioned as performed for electromigration testing. 240-, 600-, and 1200-grit silicon carbide abrasive papers were used to polish the sample exposing the mid-section surface of solder joints.

Nano-indentation was first performed directly on the cross-sectioned solder joint surface. Six indentations were made on the solder joint of Module #2. The measured values of Young's modulus by >50%. For instance, the modulus varied from 40*GPa* to 69*GPa*. The scattered measurements are intrisinc for flip chip solder joints (Basaran and Jiang 2002). However, surface preparation also contributes to scatter in measured properties.

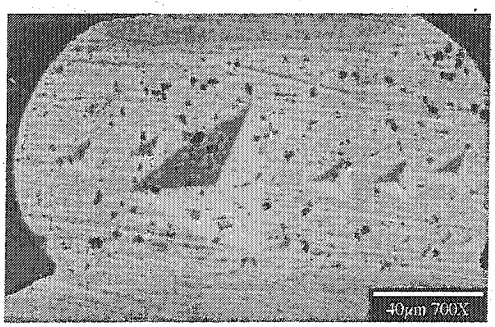


Figure 169 . SEM secondary image of solder joint of Module #2 after nano-indentation test

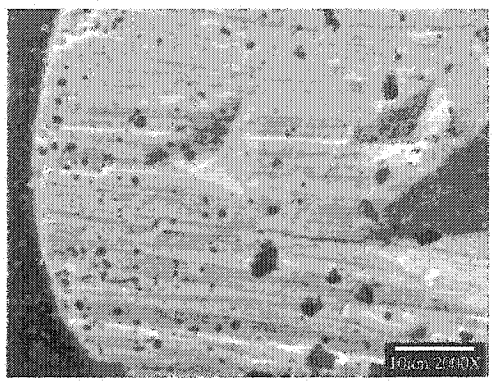


Figure 170. Large magnification SEM secondary image of solder joint of Module #2 after nano-indentation test

In instrumented indentation technique, the projected contact area needs to be calculated in order to calculate the elastic modules as describe in the previous section. The projected contact area is calculated from an empirically determined area function (Equation (5.19)) based on the measured contact depth. If the sample surface is not sufficiently flat and smooth, miscalculation of contact area may occur and lead to inaccuracy in modulus and hardness calculation. SEM imaging verified this, as shown in Figure 169 and Figure 170. There were deep scratches on the solder surface compared to the indentation depth (as small as 2000 *nm*) due to the polishing with silicon carbide paper. In the UB electronic packaging lab, plenty of nano-indentation tests were performed on BGA solder joints and consistent measurements of modulus were observed. The same surface preparation procedure was employed (240-, 600-, and 1200-grit silicon carbide paper in sequence) on those solder joints. The sizes of those solder joints are about 400-500 μm in diameter compared to 140 μm for current flip-chip solder joints. The SEM images of larger size solder joints prepared with 1200 grit silicon carbide paper yielded much smoother surface. Therfore, we think that although the compositions of the solder joints are the same and the same surface preparation procedure was followed, poor surface preparation may occur for smaller sized flip-chip solder joints. To improve the

accuracy of the nano-indentation test and to standardize a surface preparation procedure for all the experiments, an ASTM standard was chosen. The ASTM standard E3 (1999b) was applied to the surface preparation for Module #3. First, 1200-grit abrasion was used, followed by polishing with $0.5\mu m$ gamma alumina and a final polish with $0.05\mu m$ gamma alumina. By following the ASTM E3 standard, a much better surface finish was achieved on the solder joint of Module #3, as shown in Figure 109. The modulus and hardness measurements on the finely polished solder surface of Module #3 are shown in Table 17. The average modulus is $34.7GPa$ with standard deviation of 2.52 (7.3%), and average hardness is $0.21GPa$ with deviation of 0.03 (14%).

Table 17 Nano-indentation test on Module # 3 (without current stressing)

Module#3	Young's Modulus (GPa)	Hardness (GPa)	Indentation Depth(nm)
Test 1	35.876	0.231	2000
Test 2	34.721	0.254	2000
Test 3	34.472	0.198	2000
Test 4	30.061	0.155	2000
Test 5	37.436	0.21	2000
Test 6	35.872	0.197	2000
Average	34.7	0.21	
Std Dev.	2.52	0.03	

Table 18 Nano-indentation test on Module # 1 after 37.5 hours of current stressing (without re-polishing)

Module#1	Young's Modulus (GPa)	Hardness (GPa)	Indentation Depth(nm)
Test 1	39.772	0.246	2000
Test 2	27.322	0.141	2000
Test 3	49.916	0.336	2000
Test 4	38.905	0.269	2000
Test 5	46.459	0.322	2000
Average	40.47	0.26	

Table 19 Nano-indentation test on Module # 1 after 37.5 hours of current stressing (re-polished following procedure in ASTM E3 standard)

Module #1	Young's Modulus (GPa)	Hardness (GPa)	Indentation Depth(nm)
Test 1	34.733	0.214	2000
Test 2	35.55	0.178	2000
Test 3	41.405	0.229	2000
Test 4	37.613	0.183	2000
Test 5	34.844	0.184	2000
Test 6	36.961	0.257	2000
Test 7	36.986	0.182	2000
Average	36.87	0.20	

Module #1 was taken off the circuit after 37.5 hours of 1 Amps current (the calculated current density was $8\times10^3 Amp/cm^2$) stressing for nano-indentation testing. First, nano-indentation was performed on the solder joint surface without re-polishing the surface. As shown in Figure 114(a), the cross-sectioned surface of the solder joint of Module #1 became very rough after 37.5 hours of electromigration. Largely scattered measurements on modulus (from 27.3GPa to 49.9GPa) and hardness (from 0.141GPa to 0.336GPa) were observed as expected as shown in Table 18. Then the solder joint was re-polished following the procedure in the ASTM E3 standard. The nano-indentation measurements from the re-polished solder joint of Module #1 are shown inTable 19. The average modulus for the re-polished solder joint of Module #1 is 36.87GPa. After the first set of indentation tests, the residual stress within the solder joint, due to the plastic deformation caused by indentation, may alter its mechanical properties. But since a small indentation depth of 2000*nm* was applied, the plastic deformation only existed in the region very near to the surface. When the re-polishing procedure was applied, over 5000*nm* thickness of solder was polished away from its surface; thus, the residue stress

from the first set of indentation would not affect the results from the second set of indentation.

The modulus and hardness values of current stressed Module #1 are greater than those of Module #3 which was not current stressed. This observation is contrary to the expectation that the modulus or hardness of a material would decrease as damage nucleates in the material, as observed in mechanical or thermal fatigue experiments. We think the reason underneath this observation is that although the composition of the solder joints and manufacturing processes in these two modules are assumed to be the same; there may have been initial mechanical property differences. This is verified by performing indentation tests on over 50 flip-chip solder joints without current stressing, all following ASTM E3 surface preparation procedure (Appendix A-3). The measured Young's modulus for these solder joints ranges from 27-50*GPa*, with a 95% confidence interval of 39.4-41.7*GPa*. This observation confirms the report by Basaran and Jiang (Basaran and Jiang 2002).

In the preliminary nano-indentation experiment, we found out that the surface preparation is very important for nano-indentation test on flip-chip solder joints. In later experiments, ASTM standard E3 is used as a standard surface preparation procedure for all the test modules. The initial mechanical properties of each solder joint are found to vary between different modules. Based on this finding, an improved experiment procedure is implemented in the later experiments. In the new experiment procedure, nano-indentation tests are performed on the solder joint before current stressing to obtain the initial mechanical properties. Then the solder joint is re-polished and subjected to current stressing. After a certain number of hours of current stressing, the module is taken

off the circuit and the solder joints were again re-polished. A Nano-indentation test is performed to obtain the new mechanical properties. This scheme is possible since the indentation depth is $2\mu m$ and thus only a very thin layer (several microns) needs to be polished away after indentation. After the first set of indentations, the residual stress within the solder joint, due to the plastic deformation caused by indentations, may alter its mechanical properties. However, the indentation depth was only $2\mu m$, hence the plastic deformation only existed in the region very near to the surface. When the specimen was re-polished, a solder layer several microns thick was polished away; therefore, the residual stress from the first set of indentations would not affect the results from the second set of indentations.

5.6.3 Improved Nano-indentation Experiments

In continuum damage mechanics, the damage variable, D, represents the material deterioration during various physical phenomena. For undamaged (virgin) material, $D = 0$. For damaged material, $0 < D < 1$. An effective way to measure damage is based on the influence of damage on elasticity, $\tilde{E} = E(1-D)$, where $\tilde{E}$ is effective Young's modulus of the damaged material and E is the Young's modulus of undamaged material. Thus, the values of damage may be derived from measurements of $\tilde{E}$ (Lemaitre 1996):

$$D = 1 - \frac{\tilde{E}}{E} \tag{5.21}$$

Basaran and Tang (Basaran and Tang 2003) have experimentally shown that this is the most stable criterion for quantifying the degradation of ductile solder alloys. When void nucleates in the solder joints during current stressing, the material is viewed as damaged at the mesoscale and the value of damage is proportional to the density of

microvoids. Thus we expect the measured effective Young's modulus to decrease in the area of void nucleation. Since the void nucleation is found to be localized as described in Section 5.4, the damage or the decrease in effective Young's modulus is expected to be localized. Since nano-indentation can measure the Young's modulus in an extremely small area, the localized evolution of modulus on the solder joint during current stressing can be captured. The indentation method used in the experiment is "MTS XP CSM Standard Hardness, Modulus, and Tip Calibration," where contact stiffness and, therefore, the modulus are continuously calculated by dynamic measurement techniques. This method is good for testing metal material with small volume. Loading is controlled in such a way that the indenter penetrating velocity divided by penetrating depth (defined as strain rate target) was held constant at 0.05/s. The maximum indentation depth was set to be 2000 nanometer in the tests. Figure 171 shows the load vs. displacement into surface curve for an actual indentation on one solder joint, which was directly measured by the nano-indenter (note that although this figure shows only the profile of the applied force and the displacement response from the sample, neither the contact stiffness nor modulus was calculated from this curve).

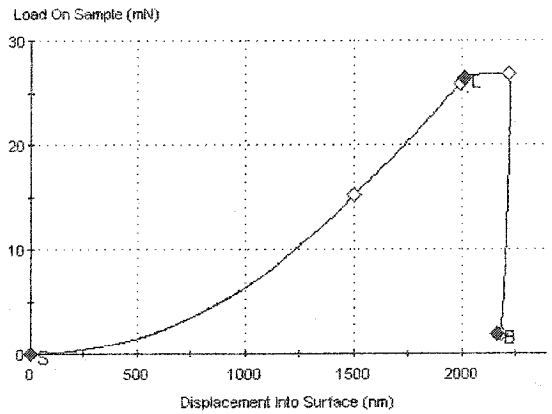


Figure 171 Load vs. Displacement into surface for an indentation

Figure 172 shows the modulus vs. displacement curve for that indentation, where the modulus was calculated based on the aforementioned theory. Since the contact stiffness, S, was continuously measured, the modulus was calculated as a continuous curve. Although the modulus is continuously measured throughout the penetration depth from 0~2000 nanometer, the reported Young's modulus is the average value over the penetration depth from 1500 to 2000 nanometer in order to eliminate any size effect or inaccuracy present at small indentation depths. Throughout our tests, the measured modulus for the majority of the solder joints follows a similar tendency: the modulus at small indentation depth is much greater than that at larger depth and decreases with indentation depth until it reaches a relatively stable value as shown in Figure 172.

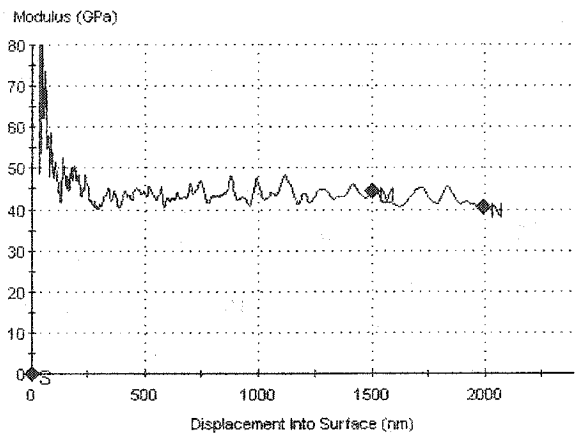


Figure 172 Modulus vs. Displacement into surface for an indentation

This observation agrees well with results of many nano-indentation size effect experiments, which has been an active research topic for many years. Strain gradient theory is the most widely used theory for explaining this phenomenon (Ning et al. 2003;Ning et al. 2003;Elmustafa and Stone 2003;Gao and Fan 2002;Gao and Fan 2002;Gerberich et al. 2002;Nix and Gao 1998). However, size effect is not the focus of

this research; therefore, an average modulus from a depth of 1500~2000 nanometers is chosen for the purpose of comparison between different stressing times.

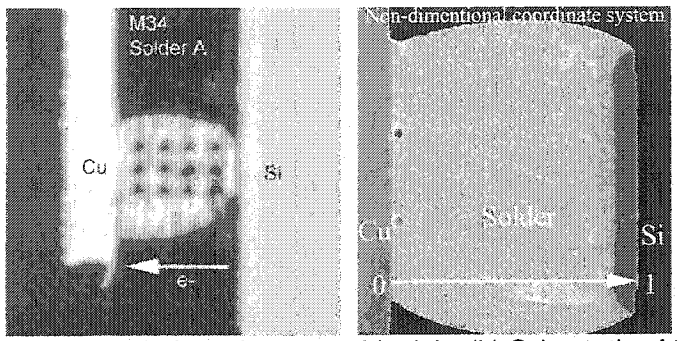


Figure 173 (a) Distributed nano-indentations on solder joint (b) Schematic of the non-dimensional Coordinate

In order to pin-point the distribution of effective Young's modulus, nano-indentations were performed on different locations on each solder joint as shown in Figure 173(a) in the experiment. In order to illustrate the distribution of Young's modulus within a solder joint, a non-dimensional coordinate system is employed. In this coordinate system, 0 denotes the interface between copper and solder and 1 denotes the interface between solder and silicon from Cu-solder interface to solder-silicon interface, as shown in Figure 173(b). Nano-indentation tests were performed on each solder joint before and after a certain amount time of current stressing in order to explore the evolution of modulus during stressing.

5.6.4 Experiment Results

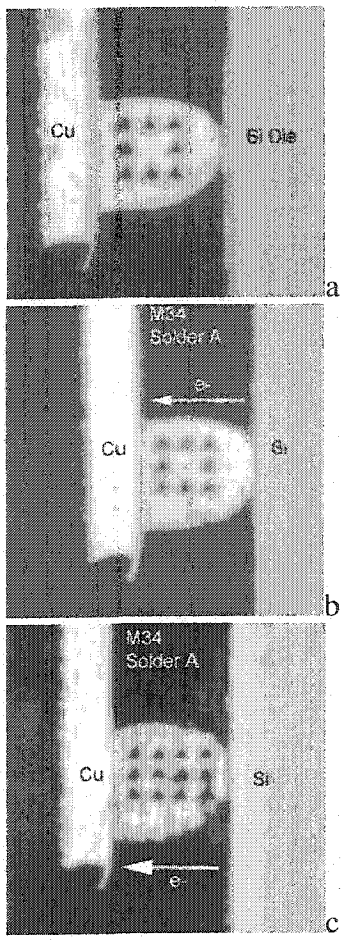


Figure 174 Nano-indentation on solder joints A of M34: (a) Initial (b) 22 hours (c) 865 hours of 0.9A current stressing

Table 20 Initial Distribution of Young's Modulus for solder joint A of M34

Position	0.20	0.41	0.61
Modulus (GPa)	46.7	44.1	42.5
	48.1	n/a	45.2
	47.7	47.1	45.0
Mean (GPa)	47.5	45.6	44.2
Total average	45.8 (GPa)		

Table 21 Distribution of Young's Modulus after 22 hours stressing for solder joint A of M34

Position	0.20	0.41	0.61
Modulus (GPa)	44.1	43.4	41.0
	49.7	n/a	44.2
	48.1	44.9	43.8
Mean (GPa)	47.3	44.2	43.0

Table 22 Distribution of Young's Modulus after 865 hours stressing for solder joint A of M34

Position	0.18	0.38	0.60	0.81
Modulus (GPa)	38.8	35.7	36.3	34.3
	42.8	39.2	43.8	35.7
	40.6	40.0	32.5	23.2
Mean (GPa)	40.7	38.3	37.5	31.1

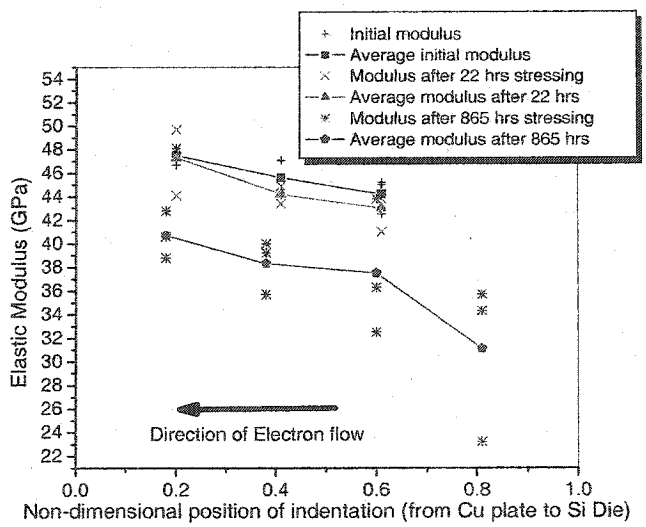


Figure 175 Evolution of elastic modulus distribution on the non-dimensional coordinate system during current stressing for solder joint A of M34

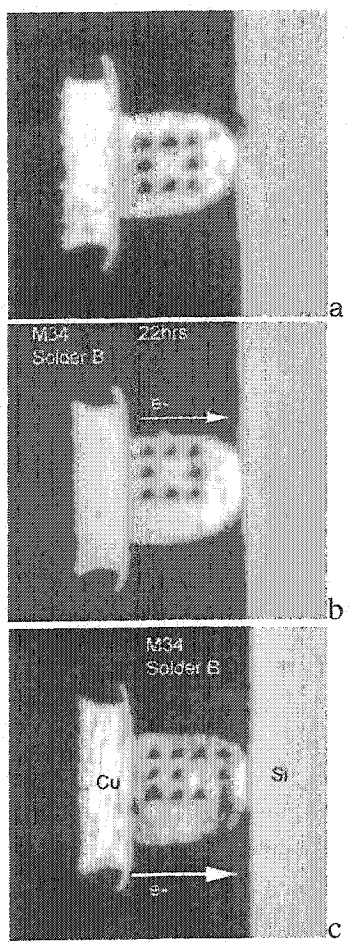


Figure 176 Nano-indentation on solder joints B of M34: (a) Initial (b) 22 hours (c) 865 hours of 0.9A current stressing

Table 23 Initial Distribution of Young's Modulus for solder joint B of M34

Position	0.23	0.43	0.64
Modulus (GPa)	50.0	48.3	46.9
	52.2	n/a	47.9
	49.9	48.5	50.0
Mean (GPa)	50.7	48.4	48.3
Total average	49.2 (GPa)		

Table 24 Distribution of Young's Modulus after 22 hours stressing for solder joint B of M34

Position	0.16	0.35	0.58
Modulus (GPa)	47.5	45.2	44.5
	51.9	n/a	43.9
	52.2	49.0	45.5
Mean (GPa)	50.5	47.1	44.6

Table 25 Distribution of Young's Modulus after 865 hours stressing for solder joint B of M34

Position	0.18	0.36	0.57	0.77
Modulus (GPa)	41.8	38.4	46.4	38.8
	45.5	37.3	n/a	n/a
	n/a	40.8	42.3	31.1
Mean	43.7	38.8	44.4	35.0

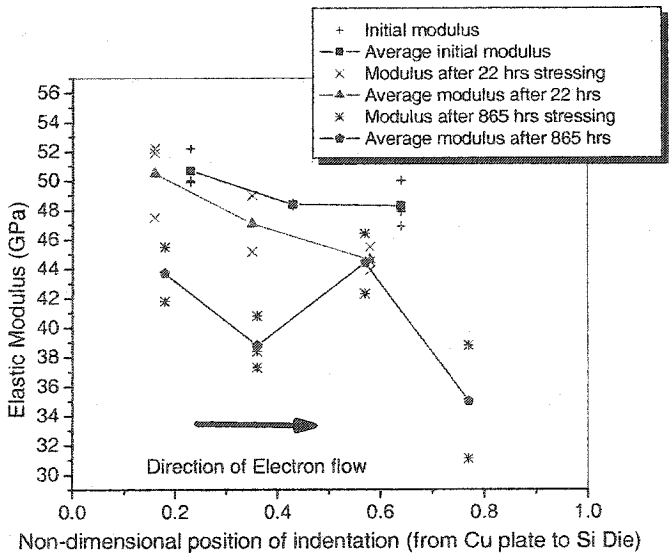


Figure 177 Evolution of elastic modulus distribution on the non-dimensional coordinate system during current stressing for solder joint B of M34

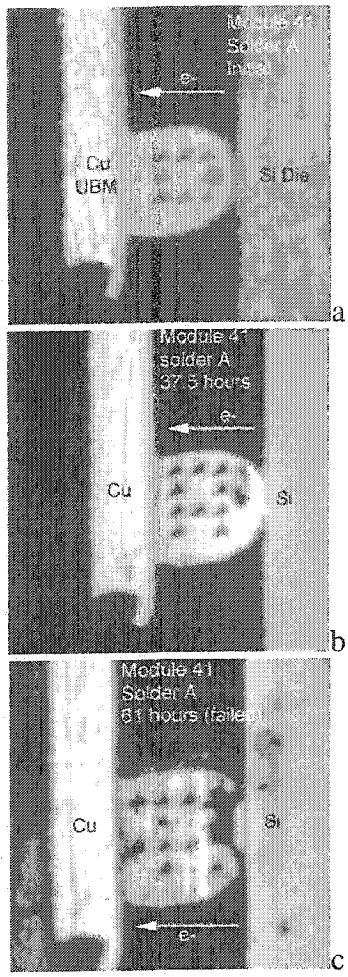


Figure 178 Nano-indentation on solder joints A of M41: (a) Initial (b) 37.5 hours (c) 61 hours of 1A current stressing

Table 26 Initial Distribution of Young's Modulus for solder joint A of M41

Position	0.33	0.52	0.75
Modulus (GPa)	39.8	43.1	n/a
	42.1	n/a	n/a
	42.2	36.5	n/a
Mean (Gpa)	41.4	39.8	n/a
Total average	40.7 (GPa)		

Table 27 Distribution of Young's Modulus after 37.5 hours stressing for solder joint A of M41 (Two indentation tests were performed after 37.5 hours of stressing for this solder joint, the photo on the left shows only one of them)

Position	0.14	0.20	0.36	0.42	0.61
Modulus (GPa)	43.5	38.4	45.6	42.5	40.8
	n/a	45	44.9	n/a	38.3
	46.9	43.8	42.4	38.1	25
	n/a	42.8	43.1	n/a	30.5
Mean (Gpa)	45.2	42.5	44	40.3	33.7

Table 28 Distribution of Young's Modulus after 61 hours stressing for solder joint A of M41

Position	0.17	0.37	0.57	0.74
Modulus (GPa)	44.8	39.7	39.6	25.5
	n/a	39.3	n/a	17.5
	52.5	38.5	25.9	n/a
	n/a	40.3	n/a	21.1
Mean (Gpa)	48.7	39.5	32.8	21.4

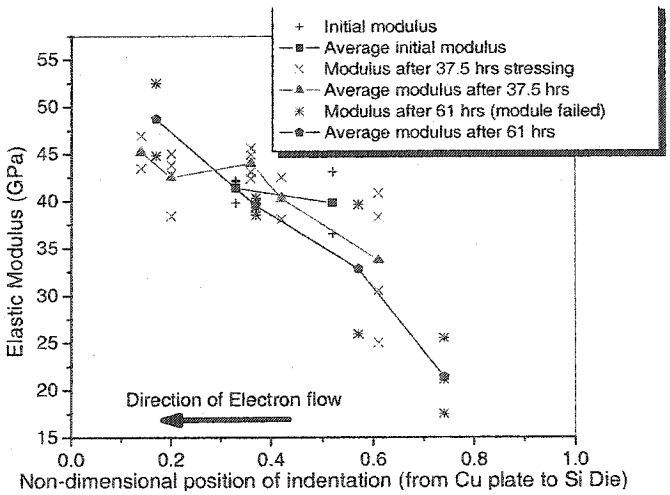


Figure 179 Evolution of elastic modulus distribution on the non-dimensional coordinate system during current stressing for solder joint A of M41

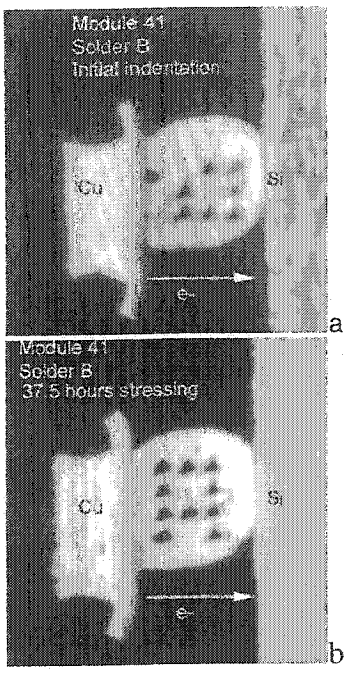


Figure 180 Nano-indentation on solder joints B of M41: (a) Initial (b) 37.5 hours [nano-indentation experiment was not performed on this solder joint after 61 hours of stressing because it was melted]

Table 29 Initial Distribution of Young's Modulus for solder joint B of M41

Position	0.33	0.55	0.76
Modulus (GPa)	n/a	43.9	39.5
	45.7	n/a	n/a
	42.7	41.4	41.9
Mean (GPa)	44.2	42.7	40.7
Total average	42.5 (GPa)		

Table 30 Distribution of Young's Modulus after 37.5 hours stressing for solder joint B of M41

Position	0.25	0.46	0.67
Modulus (GPa)	45.0	42.0	38.2
	44.5	n/a	35.3
	44.7	42.3	35.8
	41.5	n/a	40.5
Mean (GPa)	43.9	42.2	37.5

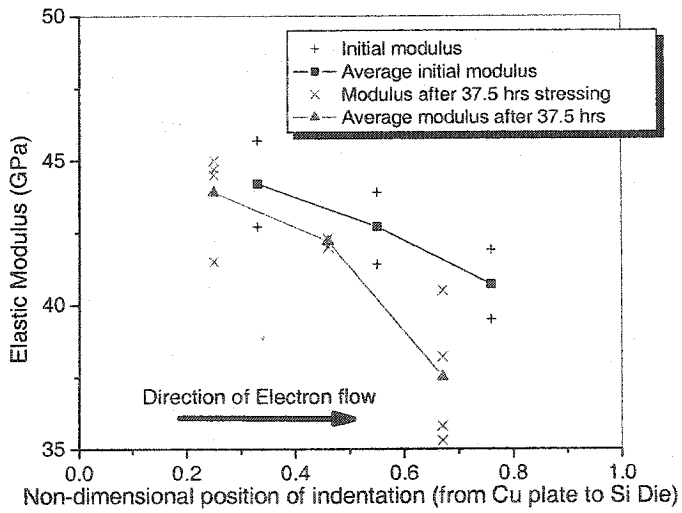


Figure 181 Evolution of elastic modulus distribution on the non-dimensional coordinate system during current stressing for solder joint B of M41

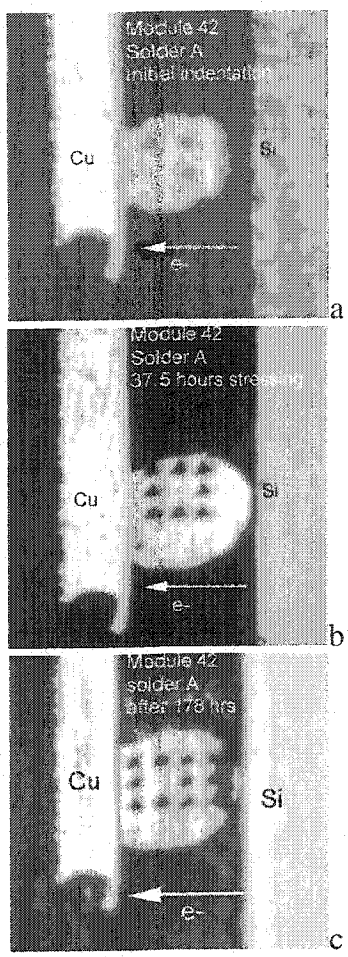


Figure 182 Nano-indentation on solder joints A of M42: (a) Initial (b) 37.5 hours (c) 178 hours of 1A current stressing

Table 31 Initial Distribution of Young's Modulus for solder joint A of M42

Position	0.22	0.50	n/a
Modulus (GPa)	43.1	39.5	n/a
	n/a	39.5	n/a
Mean (GPa)	43.1	39.5	n/a
Total average	40.7 (GPa)		

Table 32 Distribution of Young's Modulus after 37.5 hours stressing for solder joint A of M42

Position	0.17	0.38	0.58
Modulus (GPa)	41.8	42.0	40.9
	43.5	n/a	38.8
	45.9	42.7	42.2
Mean (GPa)	43.7	42.4	40.6

Table 33 Distribution of Young's Modulus after 178 hours stressing for solder joint A of M42

Position	0.15	0.36	0.56	0.76
Modulus (GPa)	41.6	39.2	36.0	24.8
	42.1	n/a	35.1	19.8
	42.6	36.8	34.9	17.5
Mean (GPa)	42.1	38	35.3	20.7

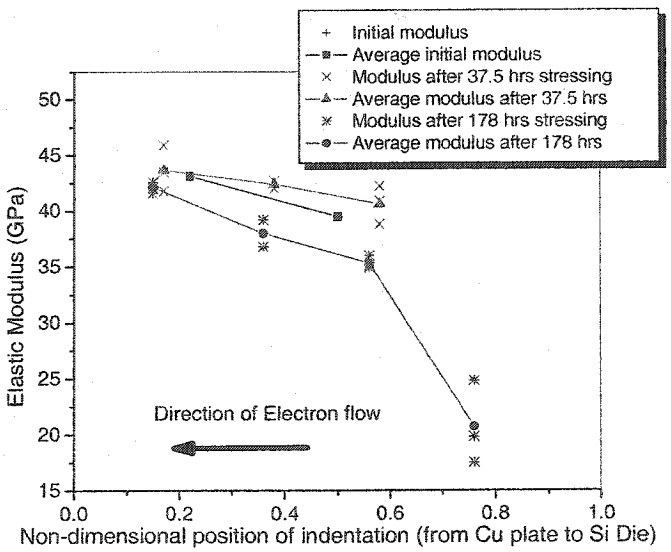


Figure 183 Evolution of elastic modulus distribution on the non-dimensional coordinate system during current stressing for solder joint A of M42

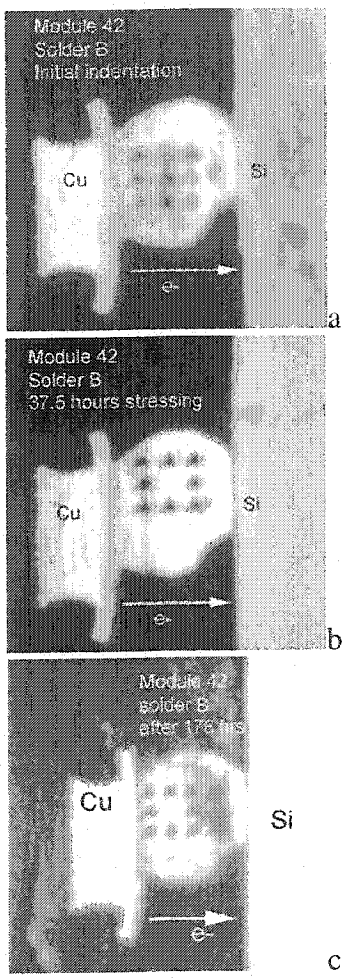


Figure 184 Nano-indentation on solder joints B of M42: (a) Initial (b) 37.5 hours (c) 178 hours of 1A current stressing

Table 34 Initial Distribution of Young's Modulus for solder joint B of M42

Position	0.18	0.39	0.61
Modulus	48.5	45.6	47.7
	49.9	n/a	43.9
	45.4	43.7	42.0
Mean (GPa)	47.9	44.7	44.5
Total average	45.8 (GPa)		

Table 35 Distribution of Young's Modulus after 37.5 hours stressing for solder joint B of M42

Position	0.25	0.45	0.65
Modulus	41.5	44.3	43.2
	48.3		43.9
	47.7	44.5	42.2
Mean (GPa)	45.8	44.4	42.2

Table 36 Distribution of Young's Modulus after 178 hours stressing for solder joint B of M42

Position	0.12	0.30	0.50	0.68
Modulus (GPa)	47.0	43.2	38.7	34.4
	43.5	n/a	37.9	16.4
	44.2	40.3	37.2	24.8
Mean (GPa)	44.9	41.8	37.9	25.2

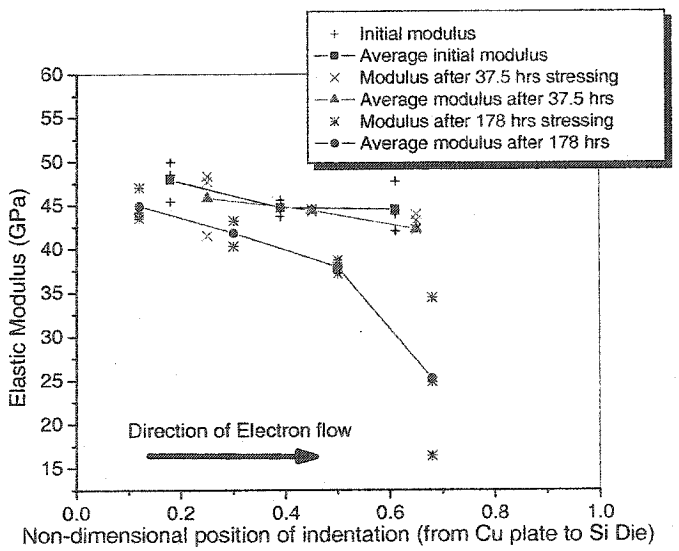


Figure 185 Evolution of elastic modulus distribution on the non-dimensional coordinate system during current stressing for solder joint B of M42

5.6.5 Discussions

In the previous section, the distribution of measured elastic modulus from nano-indentation tests for each solder joint was observed on the dimensionless coordinate before and after current stressing. Since several indentations were conducted at a single coordinate position, both the measured values and their average are shown in these tables and figures. As shown in these figures, the decrease of Young's modulus is clear for each solder joint after current stressing. In all cases, the maximum drop in modulus is always near the solder-silicon interface, no matter what the direction of electron flow. This agrees with SEM observations that indicate void nucleation is always in this region.

In the region near the Cu-solder interface (cooler side), there is no drop of modulus or the drop in modulus is considerably smaller than that in the region near solder-silicon interface (hotter side). This observation also confirms that thermomigration was actually taking the leading role during the current stressing for these solder joints, no matter what the current flow direction was. It indicates that the damage in a solder joint during current stressing is very much localized. The mechanical damage accumulates only in the regions of void nucleation. Apart from the general trend that measured modulus is always higher near the solder–cu plate interface, and lower near the solder–Si die interface, the modulus distribution of solder joint B in M34 is rather zigzag as shown in Figure 177. This anomaly could be due to the non-homogeneous diffusion or migration within this solder joint during current stressing, as discussed in Section 5.4.

Table 37 Maximum measured damage in the solder joints

Module #	Current level (A)	Stressing Temperature (°C)	Stressing time (hours)	Solder Joint	Current Density (10^4A/cm^2)	D_{max}
42	1	120	178	A	0.72	0.51
				B	0.73	0.45
41	1	150	61	A	0.96	0.48
				B	1.0	n/a
34	0.9	100	865	A	0.62	0.32
				B	0.61	0.29

n/a: Solder failed before measurement was taken

Table 37 shows the maximum measured damage as defined in Equation (5.21) in each solder joint after a certain amount time of current stressing. The effective modulus used in calculation is taken from the average measured modulus at the positions nearest to the solder–Si interface; the undamaged modulus is taken as the total average modulus from the measurements of the virgin solder joint. The module eventually failed at the end of the testing when the damaged solder joint was unable to sustain the current and thermal loading. Modules 34, 41, and 42 failed after a total of 960, 61, and 256 hours of current stressing, respectively. Table 37 clearly shows that absolute current level is not a prominent factor for mechanical degradation of solder joints. Even with current levels about the same, the solder joints in M34 still had much less D_{max} even after a much longer time of stressing. The combination of current density and stressing temperature, however, seem to control the degradation of a solder joint during current stressing. For example, solder joints in M41, which had the highest current density and stressing temperature, had the fastest mechanical degradation. This is because higher current density leads to faster electromigration; higher stressing temperature leads to greater thermomigration since higher temperature on the silicon die indicates a higher temperature gradient, as illustrated in Section 5.3. Higher temperature also leads to greater solder diffusivity, which accelerates both thermomigration and electromigration.

5.6.6 Conclusion

In this section, the nano-indentation experiment results of flip-chip solder joints under high current stressing are reported. Nano-indentation tests show that the elastic modulus of a solder joint degrades during high current stressing. The decrease of modulus or damage of solder during current stressing is localized in the area where void nucleates. The combination of current density and stressing temperature are found to be the controlling factors for the mechanical degradation of solder joints during stressing, rather than current density alone.

Chapter 6

Discussions and Conclusions

6.1 Fundamental Contributions

This dissertation studied on the reliability of microelectronics and power electronics solder joints under high density electric current stressing. Reliability of solder joints under high electric current stressing has never been a concern up to this point, because they carry low current densities. Therefore, very few studies can be found in the literature. However, it is very important for future microelectronics and power electronics systems. This dissertation provides the basic understanding of the failure mechanism, displacement measurements, and mechanical constitutive modeling of solder joints under high density current stressing.

1. The in-situ deformation evolution in BGA solder joints under high electric current density is measured with Morie Interferometry technique for the first time in the literature. We have found that the deformation in BGA solder joints created by high current density is irreversible.
2. A diffusion-mechanical coupled electromigration constitutive model is proposed for solder alloy. It is numerically implemented with FEM method to simulate the deformation evolution in Pb-free BGA solder joints under high current density

and is compared with the experimental measurements. Good agreement between the simulation and experimental results proves its effectiveness.

3. We have found that the distribution of current density in the BGA solder joints have a significant effect on the deformation in solder joint.

4. We have found that thermomigration is significant in flip-chip solder joints and is comparable to electromigration due to thermal gradient in these solder joints created by the joule heating in the silicon device.

5. We have reported the failure modes and void nucleation modes in eutectic Pb/Sn flip-chip solder joints under high electric current density. The major failure mechanism is identified as the void nucleation and growth due to the combined effects of electromigration and thermomigration.

6. We have proposed a Pb phase coarsening model for eutectic Pb/Sn flip-chip solder joints based on experimental observation.

7. We have found that elastic modulus of flip-chip solder joints degrade under high current density using nano-indentation technique.

6.2 Discussion

In the experimental part, high density current stressing experiments were conducted using flip-chip test vehicles. Electromigration is observed in these flip-chip solder joints at a current density near $1x10^4$ *amp/cm*^{2}. In addition to electromigration, thermomigration is observed in the solder joints under current stressing, because high temperature gradients are maintained in these solder joints due to joule heating in the

devices. Thermomigration may assist or counter electromigration depending on the direction of the thermal gradient and electric field, and is on the same magnitude of electromigration. This finding suggests that the reliability of flip-chip solder joints under current stressing can be improved by better thermal management.

Our experiments also identified that the major failure mechanism of flip-chip Sn63/Pb37 eutectic solder joints under high density current stressing is the void nucleation and growth due to the combined effects of electromigration and thermomigration. The Ni UBM–solder interface is the favorite site for the void nucleation and growth. The effect of pre-existing voids on the failure process of a solder joint is found to be dependent on their location. Black's equation is found not to be a reliable way to predict the lifetime of a solder joint under current stressing. This is because that different void nucleation and growth mechanisms exist in the failure process of the solder joints and the fact that Black's equation does not consider the effect of thermomigration on the lifetime of a solder joint.

Nano-indentation tests conducted on the flip-chip solder joints during stressing show that the elastic modulus of a solder joint degrades during high current stressing. The decrease of the modulus or damage of a solder joint during current stressing is localized in the area where void nucleates. Current density and stressing temperature are found to be the controlling factors for the mechanical degradation of solder joints during stressing. In the experiments, Pb Phase growth is observed under different current density and temperature. Higher current density leads to faster Pb phase coarsening. Based on the test results, a Pb phase coarsening model that includes the influence of current density is proposed: $d^n - d_0^n = Kj^m t$. The current density exponent m is found to be 3, and the phase

growth exponent n is found to be 5.5. Electric current density seems to have a greater influence on phase growth in solder joints than temperature in our test temperature range.

The Moiré Interferometry technique is used to measure the in-situ displacement evolution of BGA solder joint under electric current stressing. First, the technique is verified by a low current density stressing experiment. Later, the improved Moiré Interferometry experiments with thermal control distinguish deformations of the lead-free solder joints due to pure current stressing above 5000 A/cm^2. This is the first time in the literature the in-situ deformations of the solder joints under current stressing is reported. It is observed that high current density creates large deformation in the BGA solder joints. The experiments also suggest that this development takes several hundreds of hours since it is controlled by a diffusion-mechanical coupled process. These deformations are largely normal and transverse deformations, and the shear deformation is small. After the current is turned off, the deformations in the solder joints remain unchanged. This indicates that the deformations created by high current density are irreversible. However, these irreversible deformations are not the same as the plastic deformation. Plastic deformations are created by the high deviatoric (shear) stresses and correspond to the motion of large numbers of dislocations. The deformation created by electromigration is due to the re-arrangement of vacancies and atoms in the material as well as vacancy generations and annihilation due to diffusion and corresponds to the volumetric deformations at lattice site. However, as demonstrated in the numerical simulations, volumetric deformations at lattice sites due to electromigration give rise to high level stresses that exceed the yield stress of the solder alloy, these high deviatoric stresses may create plastic deformations. Therefore, the irreversible deformations we observed in the

experiments are the combination of electromigration deformations and plastic deformations.

In the analytical modeling part, a mechanical constitutive model for solder alloy under electromigration is presented. In this model, electromigration is viewed as a diffusion-mechanical coupled process. Volumetric strain at lattice site is assumed to be generated by vacancy migration and generation due to electromigration. This local volumetric strain is treated as an analog of thermal strain. The deformations and stresses fields are calculated as a result of local volumetric strain induced by electromigration. In this approach, the assumption of the elastic material property is not required. The constitutive model is numerically implemented into FEM code to simulate the displacement fields of the BGA lead-free solder joints under current stressing. Despite all of the assumptions and simplifications employed in the simulation, it predicts reasonably close displacement and strain results to the Moiré Interferometry experimental results in both spatial distribution and time history evolution. This indicates that the electromigration model employed in this simulation is reasonably good at predicting the mechanical behavior of lead-free solder alloy under electric current stressing. The simulation results show that the high stresses that exceed the yield stress of the solder alloy can be developed in the solder joints. This indicates that elastic assumption, which is employed by most of the researchers on electromigration, is not sufficient to model the deformation and stress evolution in solder joints under high current density. Since solder alloy is viscoplastic even at room temperature, viscoplastic model is need to model the electromigration in solder joints. However, since the electromigration model proposed in

this study does not need elastic assumption, viscoplastic constitutive model for solder alloy can be added easily.

Both the experimental observations and FEM simulation indicate that, in addition to the current density level, the current density distribution within the solder joint has a significant effect on the displacement development in the solder joint under current stressing. More specifically, larger current density non-uniformity leads to larger deformations in the solder joint in our module. This suggests that current crowding effect is important in electromigration, since it creates significant current density non-uniformity.

6.3 Suggestions for Future Work

Void nucleation and growth mechanism: Deriving a physically based void nucleation and growth model for solder joints under electro-thermo-migration will be very important for understanding, simulating, and the preventing such failures. We observed different void nucleation modes in eutectic Pb/Sn flip-chip solder joints under high current density. However, the existing void nucleation and growth theories cannot explain all these different nucleation modes. It is a complex problem that needs more studies.

Pb Phase coarsening model: This dissertation proposed a Pb phase coarsening model in eutectic Sn63/Pb37 solder joints under high electric current stressing from a phenomenological point of view. The theoretical explanations of the parameters n and m are not clear and are left for future research.

Failure modes of lead-free solder joints under current stressing: This dissertation only reported the failure modes of flip-chip Sn/Pb eutectic solder joints. Even though the lead-free solder joints are expected to have better reliabilities under current stressing (due to their higher melting points), it will be important to understand their failure modes under current stressing, because of the environmental concerns.

Damage model for solder joints under current stressing: The ultimate goal of this research project is to develop a damage mechanics model for numerical virtual testing of solder joints under current stressing. However, no damage model is proposed in this dissertation. Further work is needed to develop a damage model and to implement it into the constitutive modeling.

Implementation of viscoplastic properties into electromigration model: This dissertation used only elastic mechanical properties for solder alloys for the purpose of simplification. However, solder alloys are highly viscoplastic even at room temperature. Further work is needed to include viscoplastic behaviors so that it can be used for the simulations of the solder joints under a combined thermo-electro-mechanical loading.

Implementation of thermo-electromigration model: This dissertation proposed a thermo-electromigration model. However, it is not numerically implemented. Further work is needed to for its numerical implementation and the experimental verification.

Appendix

A-1 PlexPDE Code for Simulation of Thin Metal Film

```
{--------------------------code start here-----------------------------------------------------------}
{  Coupled_EM_Plane_Strain.PDE  }
{ ******************************************************
This problem considers the diffusional-mechanical coupled electromigration process.
The problem is modeled as a coupled PDE system.
****************************************************** }
TITLE
        'Diffusion-mechanical coupled problem in EM'
SELECT
        ERRLIM=1e-5
VARIABLES
        C(range=0,5)    {Normalized vacancy concentration}
        U(0.0000001)        {displacement in x direction}
        V(0.0000001)        {displacement in y direction}
        ev(0.001)       {volumetric strain due to EM}
DEFINITIONS
        concs = 6.02e15         {Equilibrium vacancy concentration at stress-fress state,  atom/cm**3}
        D = 2.7e-6              {diffusivity, cm**2/s}
        conc = concs*C  {vacancy concentration}
        omega=1.66e-23          {atomic volume, cm**3}
```

```
f=0.6                {average vacancy relaxation factor}
ts=1.8e-3            {vacnacy reconination relaxation time, s}
Tp=473               {operating temperature, K}
E=6.6e6              { Youngs modulus, N/cm**2}
nu=0.3496            { Poisson's Ratio  }
k=8.62e-5            { boltzman's constant, eV/K}
k1=1.38e-21          {bltzman's constant, N*cm/K}
Z=4                  {effective vacancy charge number}
ro=1.139e-8*Tp-2.07e-7      {resistivity of bulk Al, omega*cm}
j=1e6                       {Amp/cm**2, current density}
alfa=Z*ro*j/(k*Tp)
G = E/((1+nu)*(1-2*nu))
C11 = G*(1-nu)
C12 = G*nu
b = G*(1+nu)
C22 = G*(1-nu)
C33 = G*(1-2*nu)/2
{ Strains }
ex = dx(U)
ey = dy(V)
gxy = dy(U) + dx(V)
{stress}
Sx  =  C11*ex + C12*ey - b*ev
Sy  =  C12*ex + C22*ey - b*ev
Txy =  C33*gxy
Sz  =  nu*(Sx+Sy)-E*ev
sigma=((1+nu)*(Sx+Sy)-E*ev)/3      {spherical part of stress tensor}
I1=Sx+Sy+Sz                 {first invarient of stress tensor}
```

I2=Sx*Sy+Sy*Sz+Sx*Sz-Txy*Txy {second invarient of stress tensor}

vonMises=sqrt(-2/3*(I2-I1*I1/3)+1e-10)

(Balzer and Sigvaldason 1979)

Ce=concs*exp((1-f)*omega*sigma/(k1*Tp))

Gv= -(conc-Ce)/ts {vancancy generation rate}

{vancany flux}

Q=-D*(grad(C)-VECTOR(alfa*C,0)+C*f*omega*grad(sigma)/(k1*Tp))

divQ=div(Q)*concs

{Geometris}

Len=0.00500 {line length in cm}

width=0.0015 {line width in cm}

INITIAL VALUES

C = 1

U = 0

V = 0

EQUATIONS

-div(Q)+Gv/concs= dt(C)

dx(Sx) + dy(Txy) = 0 { the U-displacement equation }

dx(Txy) + dy(Sy) = 0 { the V-displacement equation }

dt(ev)=omega*(f*div(Q)*concs+(1-f)*Gv)/3

BOUNDARIES

region 1

start(0,0)

natural(C) = 0

value(U)=0

value(V)=0

line to (len,0)

natural(C) = 0

```
    value(U)=0
    value(V)=0
  line to (len,width)
    natural(C) = 0
    value(U)=0
    value(V)=0
  line to (0,width)
    natural(C) = 0
    value(U)=0
    value(V)=0
  line to finish
TIME 0 TO 6000000 BY 6000
PLOTS
    for t=0 by 0.005 to 0.02 by 0.5 to 1 by 5 to 10 by 60 to 120 by 1200 to 3600 by 7200 to 36000 by
    14400 to 72000 by 36000 to 72000 by 72000 to 360000 by 360000 to 1500000 by 1500000 to
    endtime
    elevation(C) from (0,width/2) to (len,width/2)
    elevation(magnitude(q)) from (0,width/2) to (len,width/2)
    elevation(divQ) from (0,width/2) to (len,width/2)
    elevation(sigma) from (0,width/2) to (len,width/2) as "spherical stress"
    elevation(vonMises) from (0,width/2) to (len,width/2)
    elevation(ev) from (0,width/2) to (len,width/2)
    elevation(ex,ey,gxy) from (0,width/2) to (len,width/2)
    vector(q)
    contour(u)
    contour(v)
    contour(ex)
    contour(ey)
```

```
        contour(gxy)
        contour(sigma)
        elevation(u,v) from (0,width/2) to (len,width/2)
        contour(sx)
        contour(sy)
        contour(txy)
        contour(vonMises)
        grid(x+10*U,y+10*v)
HISTORIES
        history(C) at (0,width/2) (len,width/2)
        history(sigma) at (0,width/2) (len,width/2)
        history(vonMises) at (0,width/2) (len,width/2)
END
{----------------------------end of code-----------------------------------------------------------}
```

A-2 PlexPDE Code for Simulation For Module M-Pbree-3

```
{----------------------------start of code---------------------------------------------------------}
TITLE
        'Diffusion-mechanical coupled EM problem in solder joint'
SELECT
        ERRLIM=1e-5
VARIABLES
        C(range=0,2)    {Normalized vacancy concentration}
        U(0.0001)       {displacement in x direction}
        V(0.0001)       {displacement in y direction}
        ev(0.01)        {volumetric strain due to EM}
        definitions
```

```
        concs = 1.11E+18          {equilibrium vacancy concentration at stress free state, atom/cm**3 }
        D=1.0e-6                  { diffusivity cm**2/s}
        conc = concs*C   {vacancy concentration}
        omega=2.71E-23            {atomic volume cm**3}
        f=0.6                     {average vacancy relaxation factor}
        ts=1.8e-3                 {vacnacy reconbination relaxation time s}
        Tp=303                    {operating temperature K}
        E=4.14e6                  { Youngs modulus N/cm**2}
        nu=0.33                   { Poisson's Ratio  }
        k=8.62e-5                 { boltzman's constant eV/K}
        k1=1.38e-21               {boltzman's constant N*cm/K}
        Z=20      {effective vacancy charge number}
        ro=1.15e-5      {resistivity of bulk Al, omega*cm}
        j                         {Amp/cm**2, current density}
        alfa=Z*ro*j/(k*Tp)
        G = E/(1-nu*nu)
        C11 = G
        C12 = G*nu
        b = G*(1+nu)
        C22 = G
        C33 = G*(1-nu)/2
{ Strains }
        ex = dx(U)
        ey = dy(V)
        gxy = dy(U) + dx(V)
{stress}
        Sx  =  C11*ex + C12*ey - b*ev
        Sy  =  C12*ex + C22*ey - b*ev
```

```
Txy = C33*gxy


sigma=(Sx+Sy)/3     { spherical part of stress tensor}

Ce=concs*exp((1-f)*omega*sigma/(k1*Tp))     (Balzer and Sigvaldason 1979)

Gv= -(conc-Ce)/ts          {vancancy generation rate}

Q=-D*(grad(C)-VECTOR(0,alfa*C)+C*f*omega*grad(sigma)/(k1*Tp))   {vancany flux}

dev=omega*(f*div(Q)*concs+(1-f)*Gv)/3


{Geometris}

Width_solder=0.1

height_Lowersolder=0.03

height_MidSolder=0.06

height_UpperSolder=0.06

Height_solder=height_Lowersolder+height_MidSolder+height_UpperSolder

Height_copper=0.08

Width_ext=0.1

Width_UpperCopper=1

Width_LowerCopper=0.8

INITIAL VALUES

C = 1

U = 0

V = 0

ev=0

EQUATIONS

0-div(Q)+Gv/concs= dt(C)

dx(Sx) + dy(Txy) = 0   { the U-displacement equation }

dx(Txy) + dy(Sy) = 0   { the V-displacement equation }

dt(ev)=dev
```

```
BOUNDARIES

region 1 {Lower Solder}
        MESH_SPACING =width_solder/6
        j=-11200/(1+2.5*((y-0.05)/0.10)^2)          {Amp/cm**2, current density}

  start(0,0)
  line to (width_solder,0)
        natural(C)=0
  line to (width_solder,height_LowerSolder)
  line to (0,height_LowerSolder)
        natural(c)=0
  line to finish

Region 2 {middle solder}
        MESH_SPACING =width_solder/6
        j=-11200/(1+2.5*((y-0.05)/0.10)^2)          {Amp/cm**2, current density}

  start (0, height_Lowersolder)
  Line to (width_solder, height_lowerSolder)
        natural(c)=0
  Line to (width_solder,height_lowerSolder+height_midSolder)
  Line to (0, height_lowerSolder+height_midSolder)
        natural(c)=0
  Line to finish

Region 3 {upper solder}
        MESH_SPACING =width_solder/6
```

```
        j=-11200/(1+2.5*((y-0.05)/0.10)^2)                {Amp/cm**2, current density}

Start(0,height_lowerSolder+height_midSolder)
Line to (width_solder, height_lowerSolder+height_midSolder)
        natural(c)=0
Line to (width_solder, height_lowerSolder+height_midSolder+height_UpperSolder)
Line to (0, height_lowerSolder+height_midSolder+height_UpperSolder)
        natural(c)=0
Line to finish

Region 4 {Upper Copper plate}
        j= 0                        {Amp/cm**2, current density}
        E=11.7e6
        G = E/((1.+nu)*(1.-2.*nu))
        C11 = G*(1-nu)
        C12 = G*nu
        C22 = G*(1-nu)
        C33 = G*(1-2*nu)/2
        b = G*(1+nu)
        D=1.15e-30
        Sx  =  C11*ex + C12*ey
        Sy  =  C12*ex + C22*ey
        Txy =  C33*gxy
        dev=0

start(-Width_UpperCopper,Height_solder)
        natural(c)=0
```

```
Line to (0,Height_solder)
Line to (Width_solder, Height_solder)
        natural(c)=0
Line to (width_solder+width_ext, Height_solder)
Line to (width_solder+width_ext, Height_solder+Height_copper)
Line to (-Width_UpperCopper, Height_solder+Height_copper)
        Value(U)=0
      Value(v)=0
Line to finish

Region 5 {Lower Copper plate}
        E=11.7e6
        G = E/((1.+nu)*(1.-2.*nu))
        C11 = G*(1-nu)
        C12 = G*nu
        C22 = G*(1-nu)
        C33 = G*(1-2*nu)/2
        b = G*(1+nu)

        Sx  =  C11*ex + C12*ey
        Sy  =  C12*ex + C22*ey
        Txy =  C33*gxy
        dev=0
        D=1.15e-30
        j=0                          {Amp/cm**2, current density}

Start (width_solder+width_lowerCopper,-height_copper)
   value(u)=0
```

value(v)=0

Line to (width_solder+width_lowerCopper,0)

nobc(u)

nobc(v)

line to (width_solder,0)

Line to (0,0)

Line to (-width_ext,0)

Line to (-width_ext,-height_copper)

line to finish

TIME 0 TO 9000000 BY 600

PLOTS

FOR t=0 **BY** 0.0001 **TO** 0.002 **BY** 0.05 **TO** 1 **BY** 60 **TO** 600 **BY** 600 **TO** 3000 **BY** 3000 **TO** 36000 **BY** 36000 **TO** 360000 **BY** 360000 **TO ENDTIME**

ELEVATION(u,v) from (Width_solder/2,-height_copper) to (Width_solder/2, height_copper + height_Solder) Report VAL (v,width_solder/2,height_solder)-VAL(v, width_solder/2,0)

ELEVATION(c) from (Width_solder/2,-height_copper) to (Width_solder/2, height_copper + height_Solder)

ELEVATION(div(Q)) from (Width_solder/2,-height_copper) to (Width_solder/2, height_copper + height_Solder)

CONTOUR(ev) zoom (-0.135+width_solder/2,-height_copper, height_copper*2 + height_solder, height_copper*2 + height_solder) Painted

CONTOUR(sigma) zoom (-0.135+width_solder/2,-height_copper, height_copper*2 + height_solder, height_copper*2+height_solder) painted

VECTOR(q) zoom (-0.135+width_solder/2,-height_copper, height_copper*2 + height_solder,height_copper*2 + height_solder)

CONTOUR(Sx) zoom (-0.135+width_solder/2,-height_copper, height_copper*2 + height_solder, height_copper*2+height_solder) Painted

CONTOUR(Sy) zoom (-0.135+width_solder/2,-height_copper, height_copper*2 + height_solder, height_copper*2+height_solder) Painted

CONTOUR(Txy) zoom (-0.135+width_solder/2,-height_copper, height_copper*2 + height_solder, height_copper*2+height_solder) Painted

CONTOUR(ex) zoom (-0.135+width_solder/2,-height_copper, height_copper*2 + height_solder,height_copper*2+height_solder) Painted

CONTOUR(ey) zoom (-0.135+width_solder/2,-height_copper, height_copper*2 + height_solder,height_copper*2+height_solder) Painted

CONTOUR(Gxy) zoom (-0.135+width_solder/2,-height_copper, height_copper*2 + height_solder,height_copper*2+height_solder) Painted

GRID(x+100*U,y+100*v)

CONTOUR(u) zoom (-0.135+width_solder/2,-height_copper, height_copper*2 + height_solder,height_copper*2+height_solder)

CONTOUR(v) zoom (-0.135+width_solder/2,-height_copper, height_copper*2 + height_solder,height_copper*2+height_solder)

HISTORIES

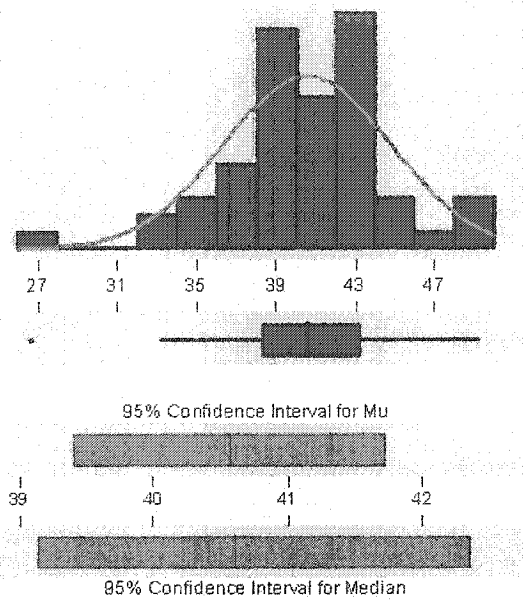
HISTORY(C) at (width_solder/2,0) (width_solder/2,height_solder)

HISTORY(VAL(v,width_solder/2,height_solder)-VAL(v,width_solder/2,0))

END

{----------end of code----------}

A-3 Initial indentation results for flip-chip solder joints



Variable: Modulus(GPa)

Anderson-Darling Normality Test

A-Squared:	0.412
P-Value:	0.330
Mean	40.5648
StDev	4.2101
Variance	17.7253
Skewness	-3.7E-01
Kurtosis	1.38604
N	54
Minimum	26.7000
1st Quartile	38.3750
Median	40.6000
3rd Quartile	43.2250
Maximum	49.2000

95% Confidence Interval for Mu

39.4157	41.7140

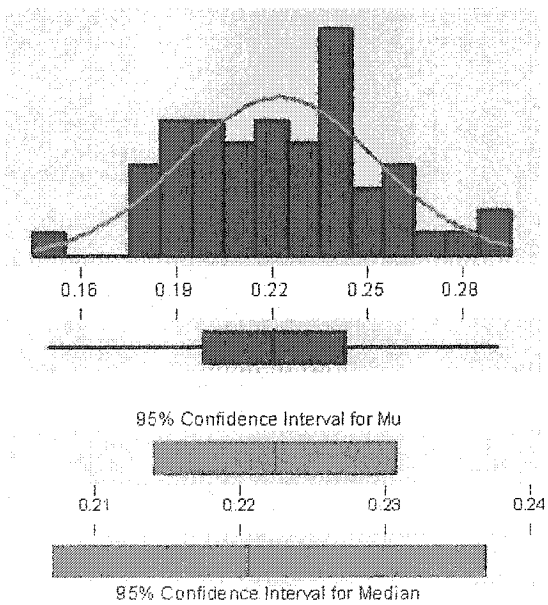
95% Confidence Interval for Sigma

3.5382	5.1975

95% Confidence Interval for Median

39.1357	42.3573

Figure 186 Elastic modulus distribution of 54 unstressed solder joints



Variable: Hardness GPa

Anderson-Darling Normality Test

A-Squared:	0.346
P-Value:	0.469
Mean	0.222352
StDev	0.030665
Variance	9.40E-04
Skewness	0.169572
Kurtosis	-3.3E-01
N	54
Minimum	0.150000
1st Quartile	0.198500
Median	0.220500
3rd Quartile	0.243250
Maximum	0.281000

95% Confidence Interval for Mu

0.213982	0.230722

95% Confidence Interval for Sigma

0.025778	0.037856

95% Confidence Interval for Median

0.207000	0.236929

Figure 187 Hardness distribution of 54 unstressed solder joints

A-4 Plane stress formulation for the elastic mechanical stress-strain model

This section gives the plane stress formulation for the electromigration constitutive model. The standard strain (ε_{ij}) – displacement (u,v,w) relationship is given by:

$$\varepsilon_x = \frac{\partial u}{\partial x}, \varepsilon_y = \frac{\partial v}{\partial y}, \varepsilon_z = \frac{\partial w}{\partial z} \tag{A.1}$$

$$\gamma_{xy} = \frac{\partial u}{\partial y} + \frac{\partial v}{\partial x}, \gamma_{xz} = \frac{\partial u}{\partial z} + \frac{\partial w}{\partial x}, \gamma_{yz} = \frac{\partial v}{\partial z} + \frac{\partial w}{\partial y} \tag{A.2}$$

With plane stress assumption, $\sigma_z = \tau_{xz} = \tau_{yz} = 0$. The constitutive relationship with the mechanical, thermal and electric current loadings is:

$$\varepsilon_x = \frac{1}{E}\{\sigma_x - v\sigma_z\} + \alpha\Delta T + \frac{\varepsilon^{elec}}{3} \tag{A.3}$$

$$\varepsilon_y = \frac{1}{E}\{\sigma_y - v\sigma_x\} + \alpha\Delta T + \frac{\varepsilon^{elec}}{3} \tag{A.4}$$

$$\varepsilon_z = -\frac{1}{E}v(\sigma_x + \sigma_y) + \alpha\Delta T + \frac{\varepsilon^{elec}}{3} \tag{A.5}$$

$$\gamma_{xy} = \frac{1}{G}\tau_{xy}, \gamma_{xz} = 0, \gamma_{yz} = 0 \tag{A.6}$$

where E is Young's modulus

v is Poisson's ratio

α is the coefficient of thermal expansion

Then

$$\sigma_x = \frac{E}{1-v^2}(\varepsilon_x + v\varepsilon_y) - \frac{E}{1-v}(\alpha\Delta T + \frac{1}{3}\varepsilon^{elec})] \tag{A.7}$$

$$\sigma_y = \frac{E}{1-\nu^2}(\varepsilon_y + \nu\varepsilon_x) - \frac{E}{1-\nu}(\alpha\Delta T + \frac{1}{3}\varepsilon^{elec}) \tag{A.8}$$

$$\tau_{xy} = G\gamma_{xy} \tag{A.9}$$

And the hydrostatic stress can be calculated as:

$$\sigma = \frac{\sigma_x + \sigma_y + \sigma_z}{3} = \frac{\sigma_x + \sigma_y}{3} \tag{A.10}$$

where $\dot{\varepsilon}^{elec}$ is coupled with the vacancy diffusion,

$$\dot{\varepsilon}^{elec} = \Omega[f\vec{\nabla}\cdot\vec{q} + (1-f)G] \tag{A.11}$$

Quasi-static mechanical equilibrium equations for plane strain problem are given by

$$\frac{\partial\sigma_x}{\partial x} + \frac{\partial\tau_{xy}}{\partial y} = 0 \tag{A.12}$$

$$\frac{\partial\tau_{xy}}{\partial x} + \frac{\partial\sigma_y}{\partial y} = 0 \tag{A.13}$$

Thus, by solving the coupled diffusion-mechanical equations (vacancy diffusion equation (3.3), volumetric strain evolution equation (A.11), and quasi-static mechanical equilibrium equations (A.12) and (A.13)), the stress evolution during electromigration can be obtained.

References

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